

DS26519DK 16-Port T1/E1/J1 Transceiver Demo Kit

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GENERAL DESCRIPTION

The DS26519DK is an easy-to-use evaluation board for the DS26519 16-port T1/E1/J1 transceiver. The DS26519DK is a stand-alone system. The board comes complete with a transceiver, transformers, termination resistors, configuration jumpers, network connectors, processor, RS-232 interface, and power adapter. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs support GPIO pins to indicate status, and FPGAs provide for multiple clock and signal routing configurations.

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DEMO KIT CONTENTS

DS26519DK Board
CD_ROM Including:
ChipView Software
DS26519 Definition Files
DS26519DK Definition File
DS26519DK Data Sheet
DS26519 Data Sheet

FEATURES

- Demonstrates Key Functions of DS26519 T1/E1/J1 SCT
- Network Connectors, Transformers, and Termination Ease Connectivity
- Careful Layout Provides Signal Integrity
- On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS26519 Register Set
- Software-Controlled (Register Mapped) Configuration Switches Facilitate Clock and Signal Routing
- All System-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs Programmed via GPIO Pins Provide Status
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

ORDERING INFORMATION

PART	DESCRIPTION
DS26519DK	Demo kit for DS26519

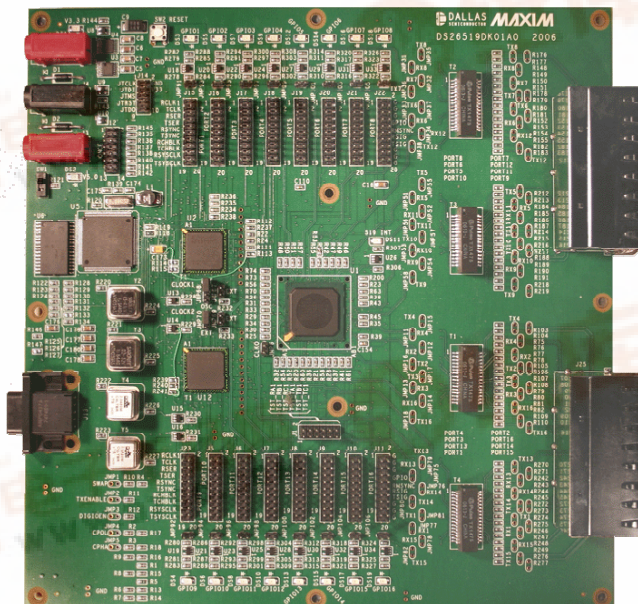


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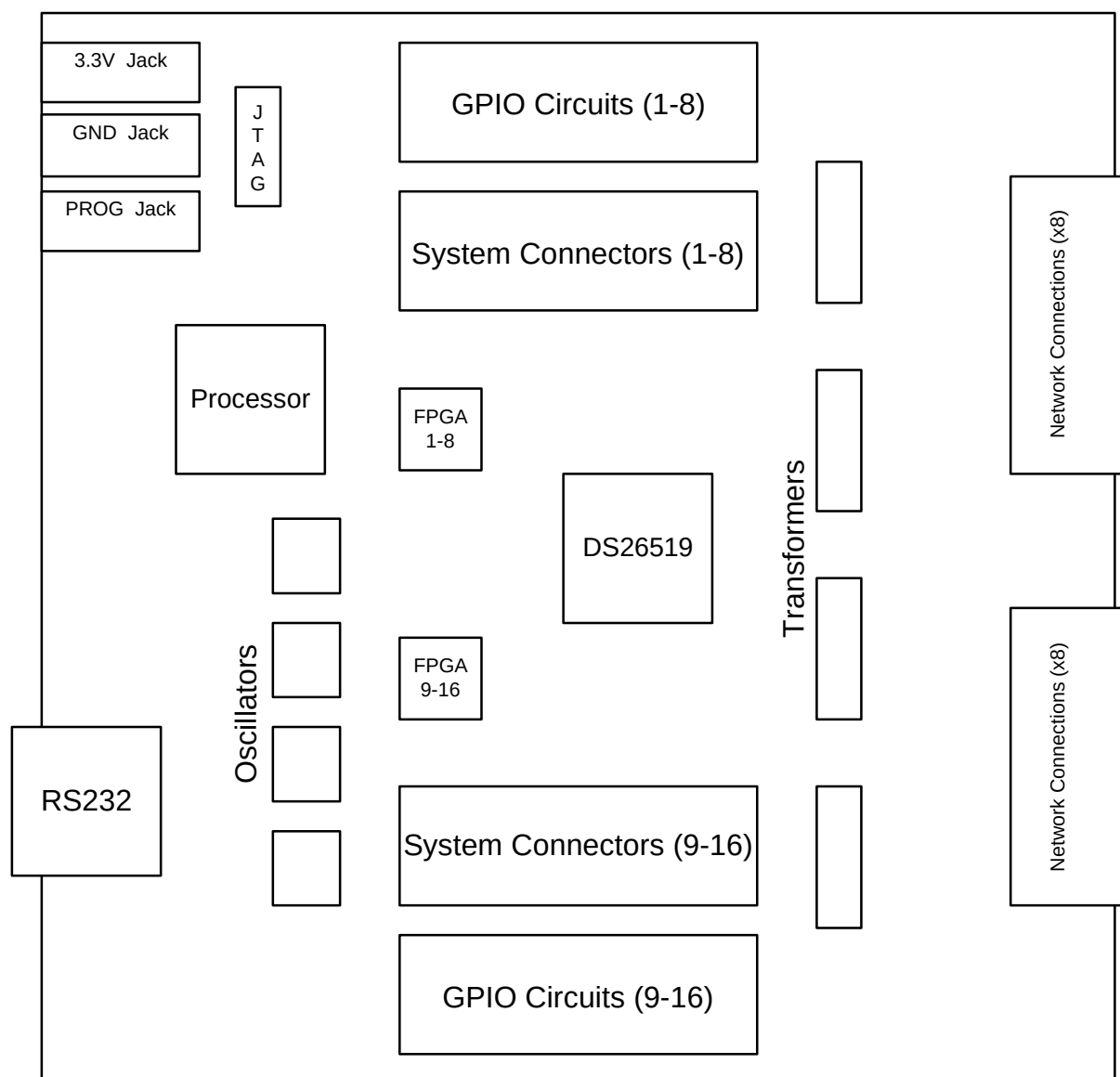
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1. BOARD FLOORPLAN

Figure 1 shows the floor plan of the DS26519DK. The DS26519 is near the center of the board. The network connections are provided on the right side of the board, which includes transformers and stacked RJ48 connectors. Toward the center of the board are two FPGAs that provide muxes for control of system-side connections via memory-mapped registers. Above and below the DS26519 are headers that provide access to all system-side signals. The GPIO circuits next to the system connectors provide an interface to the GPIO pins via a header and an LED for each GPIO. The power-supply connections, microprocessor, and JTAG connection are all in the top left quadrant of the board. The power-supply section has three banana jacks for 3.3V, ground, and programming (used at the factory). The bottom left quadrant of the board houses a serial port connector for interface to a computer and clock distribution circuitry.

Figure 1-1. DS26519DK Board Floorplan



2. [查询"DS26519DK"供应商](#) **CLOCK JUMPERS**

Jumpers JMP68 and JMP70 (middle left of board) select the main clock source for ports 1–8 and ports 9–16, respectively. The source can be external via JMP67 (ports 1–8) or JMP69 (ports 9–16) or on-board oscillators Y2 (ports 1–8) and Y3 (ports 9–16). Oscillators Y4 and Y5 are auxiliary oscillators for ports 1–8 and ports 9–16, respectively. The clock sources are muxed to the DS26519DK oscillators via FPGAs (see the [ADDRESS MAP](#) section for details).

3. **LINE-SIDE CONNECTIONS**

The DS26519DK provides four octal transformers, two stacked RJ48 connectors, and test points to support all 16 ports. The test points are clearly labeled on both sides of the transformers with port numbers.

4. **SYSTEM CONNECTORS**

System-side signals can be accessed from 16 headers. The headers are clearly labeled with port and signal information.

5. **MICROCONTROLLER**

The microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS26519 and the FPGAs.

6. **POWER-SUPPLY CONNECTORS**

Connect a 3.3V power supply across the red J2 and black J4 (GND) banana jacks for normal operation. Banana jack J3 is used by the factory for application of programming voltage for the microcontroller. Diodes D1 and D2 provide protection against power connection reversal. The LED DS1 provides indications that a 3.3V supply is connected properly. The 3.3V supply is regulated to supply proper voltages to various circuits on the board.

7. **CONNECTING TO A COMPUTER**

Connect a standard DB-9 serial cable between the serial port on the DS26519DK and an available serial port on the host computer. The host computer must be a Windows-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

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8. INSTALLING AND RUNNING THE SOFTWARE

ChipView is a general-purpose program that supports a number of Dallas Semiconductor demo kits. To install the ChipView software, run SETUP.EXE from the disk included in the DS26519DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS26519DK.

After installation, run the ChipView program with the DS26519DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Dallas evaluation platforms. In the active subwindow, select the 26519T1.DEF (or 26519E1.DEF) definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS26519's register map. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

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9. ADDRESS MAP

Address space begins at 0x81000000. All offsets given in the following tables are relative to 0x81000000.

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named "DS26519DK.DEF."

Table 9-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000	FPGA	Board identification and clock/signal routing
0X4000	DS26519	DS26519 registers

9.1 FPGA Register Map

Table 9-2. FPGA Register Map for FPGA 0 (U2)

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0100	BID	Read only	Board ID
0X0102	XBIDH	Read only	High Nibble Extended Board ID
0X0103	XBIDM	Read only	Middle Nibble Extended Board ID
0X0104	XBIDL	Read only	Low Nibble Extended Board ID
0X0105	BREV	Read only	Board FAB Revision
0X0106	AREV	Read only	Board Assembly Revision
0X0107	PREV	Read only	FPGA Revision
0X0108	PNUM	Read only	FPGA number
0x010a 0x010b 0x010c 0x010d 0x010e 0x010f 0x0110 0x0111	TCLKnSRC	Control	DS26519 TCLKn Source , Ports 1–8
0X0112	TSERSRC1	Control	DS26519 TSER Source, Ports 1–4
0x0113	TSERSRC2	Control	DS26519 TSER Source, Ports 5–8
0X0114	TSYNCIO	Control	DS26519 TSYNC IO, Ports 1–8
0X0115	RSYNCIO	Control	DS26519 RSYNC IO, Ports 1–8
0x0116	TSYNCSRC1	Control	DS26519 TSYNC Source, Ports 1–4
0x0117	TSYNCSRC2	Control	DS26519 TSYNC Source, Ports 5–8
0x0118	RSYNCSRC1	Control	DS26519 RSYNC source, Ports 1–4
0x0119	RSYNCSRC2	Control	DS26519 RSYNC source, Ports 5–8
0x011a	CLKDIVIDE	Control	Local sync clock divider
0x011b	SYNCSRC	Control	Sync source/Local sync clock source
0x011c	TSYSCLKSRC1	Control	DS26519 TSYSCLK Source, Ports 1–4
0x011d	TSYSCLKSRC2	Control	DS26519 TSYSCLK Source, Ports 5–8
0x011e	RSYSCLKSRC1	Control	DS26519 RSYSCLK Source, Ports 1–4
0X011f	RSYSCLKSRC2	Control	DS26519 RSYSCLK Source, Ports 5–8

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Table 9-3. FPGA Register Map for FPGA 1 (U12)

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0000	BID	Read only	Board ID
0X0002	XBIDH	Read only	High Nibble Extended Board ID
0X0003	XBIDM	Read only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read only	Low Nibble Extended Board ID
0X0005	BREV	Read only	Board FAB Revision
0X0006	AREV	Read only	Board Assembly Revision
0X0007	PREV	Read only	FPGA Revision
0X0008	PNUM	Read only	FPGA number
0x000a 0x000b 0x000c 0x000d 0x000e 0x000f 0x0010 0x0011	TCLKnSRC	Control	DS26519 TCLKn Source , Ports 9–16
0X0012	TSERSRC1	Control	DS26519 TSER Source, Ports 9–12
0x0013	TSERSRC2	Control	DS26519 TSER Source, Ports 13–16
0X0014	TSYNCIO	Control	DS26519 TSYNC IO, Ports 9–16
0X0015	RSYNCIO	Control	DS26519 RSYNC IO, Ports 9–16
0x0016	TSYNCSRC1	Control	DS26519 TSYNC Source, Ports 9–12
0x0017	TSYNCSRC2	Control	DS26519 TSYNC Source, Ports 13–16
0x0018	RSYNCSRC1	Control	DS26519 RSYNC source, Ports 9–12
0x0019	RSYNCSRC2	Control	DS26519 RSYNC source, Ports 13–16
0x001a	CLKDIVIDE	Control	Local sync
0x001b	SYNCSRC	Control	Sync source/Local sync clock source
0x001c	TSYSCLKSRC1	Control	DS26519 TSYSCLK Source, Ports 9–12
0x001d	TSYSCLKSRC2	Control	DS26519 TSYSCLK Source, Ports 13–16
0x001e	RSYSCLKSRC1	Control	DS26519 RSYSCLK Source, Ports 9–12
0X001f	RSYSCLKSRC2	Control	DS26519 RSYSCLK Source, Ports 13–16

Note: The following register descriptions are specific to FPGA0 (U2) but pertain to FPGA1 (U12). The ports that are referenced in the descriptions change from ports 1–8 to ports 9–12. CLOCK1 references change to CLOCK2 (except in the RSYCLKSRCn and TSYSCLKSRCn register, where CLOCK2 is used as a source in both FPGAs). BPCLK1 reference changes to BPCLK2.

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9.2 ID Registers

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x2.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0xa.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: FPGA REVISION (Offset = 0X0007)

PREV is read-only and displays the current FPGA code revision.

PNUM: FPGA NUMBER (Offset = 0X0008)

PNUM is read-only and displays the active FPGA number (0 or 1).

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9.3 Control Registers

Register Name: **TCLK1SRC**

Register Description: **TCLK1 SOURCE**

Register Offset: **0x010a**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK1 to OSC1_1544. An 0x0F written to this register connects TCLK1 to CLOCK1. A one written to bit RCLKn connects TCLK1 to RCLKn.

Register Name: **TCLK2SRC**

Register Description: **TCLK2 SOURCE**

Register Offset: **0x010b**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK2 to OSC1_1544. An 0x0F written to this register connects TCLK2 to CLOCK1. A one written to bit RCLKn connects TCLK2 to RCLKn.

Register Name: **TCLK3SRC**

Register Description: **TCLK3 SOURCE**

Register Offset: **0x010c**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK3 to OSC1_1544. An 0x0F written to this register connects TCLK3 to CLOCK1. A one written to bit RCLKn connects TCLK3 to RCLKn.

Register Name: **TCLK4SRC**

Register Description: **TCLK4 SOURCE**

Register Offset: **0x010d**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK4 to OSC1_1544. An 0x0F written to this register connects TCLK4 to CLOCK1. A one written to bit RCLKn connects TCLK4 to RCLKn.

[查询"DS26519DK"供应商](#)Register Name: **TCLK5SRC**Register Description: **TCLK5 SOURCE**Register Offset: **0x010e**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK5 to OSC1_1544. An 0x0F written to this register connects TCLK5 to CLOCK1. A one written to bit RCLKn connects TCLK5 to RCLKn.

Register Name: **TCLK6SRC**Register Description: **TCLK6 SOURCE**Register Offset: **0x010f**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK6 to OSC1_1544. An 0x0F written to this register connects TCLK6 to CLOCK1. A one written to bit RCLKn connects TCLK6 to RCLKn.

Register Name: **TCLK7SRC**Register Description: **TCLK7 SOURCE**Register Offset: **0x0110**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK7 to OSC1_1544. An 0x0F written to this register connects TCLK7 to CLOCK1. A one written to bit RCLKn connects TCLK7 to RCLKn.

Register Name: **TCLK8SRC**Register Description: **TCLK8 SOURCE**Register Offset: **0x0111**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK8 to OSC1_1544. An 0x0F written to this register connects TCLK8 to CLOCK1. A one written to bit RCLKn connects TCLK8 to RCLKn.

[查询"DS26519DK"供应商](#)Register Name: **TSERSRC1**Register Description: **TSER SOURCE 1**Register Offset: **0x0112**

Bit #	7	6	5	4	3	2	1	0
Name	RSER4	RSER4	RSER3	RSER3	RSER2	RSER2	RSER1	RSER1
Default	0	0	0	0	0	0	0	0

Note: A one written to either bit labeled RSER4, RSER3, RSER2, RSER1 connects TSERn with the respective RSERn pin. If both RSERn bits are written a one, TSERn is driven to a one. If both RSERn bits are written a zero, TSERn is pulled low. For example, 0x03 will drive TSER1 to a one.

Register Name: **TSERSRC2**Register Description: **TSER SOURCE 2**Register Offset: **0x0113**

Bit #	7	6	5	4	3	2	1	0
Name	RSER8	RSER8	RSER7	RSER7	RSER6	RSER6	RSER5	RSER5
Default	0	0	0	0	0	0	0	0

Note: A one written to either bit labeled RSER8, RSER7, RSER6, RSER5 connects TSERn with the respective RSERn pin. If both RSERn bits are written a one, TSERn is driven to a one. If both RSERn bits are written a zero, TSERn is pulled low. For example, 0x03 will drive TSER1 to a one.

Register Name: **TSYNCIO**Register Description: **TSYNC I/O SELECT**Register Offset: **0x0114**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC8	TSYNC7	TSYNC6	TSYNC5	TSYNC4	TSYNC3	TSYNC2	TSYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit TSYNCn makes the TSYNCn pin an output (driven by TSYNCnO). A zero written to bit TSYNCn makes TSYNCn an input.

Register Name: **RSYNCIO**Register Description: **RSYNC I/O SELECT**Register Offset: **0x0115**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC8	RSYNC7	RSYNC6	RSYNC5	RSYNC4	RSYNC3	RSYNC2	RSYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit RSYNCn makes the RSYNCn pin an output (driven by RSYNCnO). A zero written to bit RSYNCn makes RSYNCn an input.

[查询"DS26519DK"供应商](#)Register Name: **TSYNCSRC1**Register Description: **TSYNC SOURCE 1**Register Offset: **0x0116**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC4	SYNC4	RSYNC3	SYNC3	RSYNC2	SYNC2	RSYNC1	SYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects TSYNCnO to a common internal SYNC net. A one written to RSYNCn connects RSYNCn to TSYNCnO. If both RSYNCn and SYNCn are written a one, TSYNCnO is driven to a logic 1. If both RSYNCn and SYNCn are written a zero, TSYNCnO is held at zero.

Register Name: **TSYNCSRC2**Register Description: **TSYNC SOURCE 2**Register Offset: **0x0117**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC8	SYNC8	RSYNC7	SYNC7	RSYNC6	SYNC6	RSYNC5	SYNC5
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects TSYNCnO to a common internal SYNC net. A one written to RSYNCn connects RSYNCn to TSYNCnO. If both RSYNCn and SYNCn are written a one, TSYNCnO is driven to a logic 1. If both RSYNCn and SYNCn are written a zero, TSYNCnO is held at zero.

Register Name: **RSYNCSRC1**Register Description: **RSYNC SOURCE 1**Register Offset: **0x0118**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC4	SYNC4	TSYNC3	SYNC3	TSYNC2	SYNC2	TSYNC1	SYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects RSYNCnO to a common internal SYNC net. A one written to TSYNCn connects TSYNCn to RSYNCnO. If both TSYNCn and SYNCn are written a one, RSYNCnO is driven to a logic 1. If both TSYNCn and SYNCn are written a zero, RSYNCnO is held at zero.

Register Name: **RSYNCSRC2**Register Description: **RSYNC SOURCE 2**Register Offset: **0x0119**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC8	SYNC8	TSYNC7	SYNC7	TSYNC6	SYNC6	TSYNC5	SYNC5
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects RSYNCnO to a common internal SYNC net. A one written to TSYNCn connects TSYNCn to RSYNCnO. If both TSYNCn and SYNCn are written a one, RSYNCnO is driven to a logic 1. If both TSYNCn and SYNCn are written a zero, RSYNCnO is held at zero.

[查询"DS26519DK"供应商](#)Register Name: **CLKDIVIDE**Register Description: **SYNC CLOCK DIVIDER**Register Offset: **0x011a**

Bit #	7	6	5	4	3	2	1	0
Name	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Note: The SYNC SOURCE clock is divided by the value in this register to provide a local sync. For instance, for T1 a divisor of 193 is appropriate (C1H)

Register Name: **SYNCSRC**Register Description: **LOCAL SYNC CLOCK SOURCE AND NET SYNC SOURCE**Register Offset: **0x011b**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC1	RSYNC1	LOCAL	LOCAL	BPCLK1	OSC1	CLOCK1	CLOCK1
Default	0	0	0	0	0	0	0	0

Note: A one written to the upper nibble connects internal net (sync) to respective source. A one written lower nibble connects local sync generator to respective clock. Bit named LOCAL is a locally generated sync.

Register Name: **TSYSCLKSRC1**Register Description: **TSYSCLK SOURCE 1**Register Offset: **0x011c**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to TSYSCLK4, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to TSYSCLK3, TSYSCLK2, and TSYSCLK1, respectively. CLOCK2 comes from FPGA1.

Register Name: **TSYSCLKSRC2**Register Description: **TSYSCLK SOURCE 2**Register Offset: **0x011d**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to TSYSCLK8, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to TSYSCLK7, TSYSCLK6, and TSYSCLK5, respectively. CLOCK2 comes from FPGA1.

[查询"DS26519DK"供应商](#)Register Name: **RSYSCLKSRC1**Register Description: **RSYSCLK SOURCE 1**Register Offset: **0x011e**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to RSYCLK4, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to RSYCLK3, RSYCLK2, and RSYCLK1, respectively. CLOCK2 comes from FPGA1.

Register Name: **RSYSCLKSRC2**Register Description: **RSYSCLK SOURCE 2**Register Offset: **0x011f**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to RSYCLK8, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to RSYCLK7, RSYCLK6, and RSYCLK5, respectively. CLOCK2 comes from FPGA1.

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10. ADDITIONAL INFORMATION/RESOURCES

10.1 DS26519 Information

For more information about the DS26519, refer to the DS26519 data sheet at www.maxim-ic.com/DS26519.

10.2 DS26519DK Information

For more information about the DS26519DK including software downloads, refer to the DS26519DK Quick View page at www.maxim-ic.com/DS26519DK.

10.3 Technical Support

For additional technical support, go to www.maxim-ic.com/support.

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11. COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C174, C175	2	L_0603 CERAM 22pF 25V 5% NPO	AVX	06033A220JAT
C19, C20, C21, C24-C30, C32-C73, C75-C78, C80-C97, C99-C102, C104-C172, C193-C195	150	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
Y2-Y5	4	SOCKET, OSCILLATOR, HALF SIZE, 4-PIN THROUGH-HOLE	ARI	110880
J4	1	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	MSR	164-6218
J2, J3	2	SOCKET, BANANA PLUG, HORIZONTAL, RED	MSR	164-6219
D1, D2	2	DIODE 1A 50V GEN PURPOSE SILICON	GEN	1N4001
J13	1	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
R6-R9, R19, R22, R24, R75-R90, R95-R115, R134, R143, R144, R146, R148-R163, R168-R199, R204-R223, R237-R257, R262-R277	153	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F
U6, U7	2	IC, SRAM, 128K X 8, 32 PIN SOIC	CYP	CY62128VL-70SC
U11	1	DUAL RS232 XMTR/RCVR 16 PIN SOIC (300 MIL)	DAL	DS232AS
Y1	1	XTAL, LOW PROFILE, 8.000MHZ	ECL	EC1-8.000M
C1-C4, C181-C192	16	0805 CERAM 560pF 50V 5% NPO	PAN	ECJ-2VC1H561K
C7,C8	2	1206 CERAM 6.8uF 6.3V 10% X5R	PAN	ECJ-3YB0J685K
C10-C18, C22, C23, C31, C74, C79, C98, C103, C176-C180	21	L_1206 CERAM 10uF 10V 20%	PAN	ECJ-3YB1A106M
C5,C6	2	1206 CERAM 4.7uF 25V 10% X5R	PAN	ECJ-3YB1E475K
C9	1	L_D CASE TANT 68uF 16V 20%	PAN	ECS-T1CD686R
C173	1	L_B CASE TANT 10uF 16V 20%	PAN	ECS-T1CX106R
R20	1	RES 0603 10.0K Ohm 1/16W 1%	PAN	ERJ-3EKF1002V
R91-R94, R164-R167, R200-R203, R258-R261	16	RES 0603 121 Ohm 1/16W 1%	PAN	ERJ-3EKF1210V
R120	1	RES 0603 33.2 Ohm 1/16W 1%	PAN	ERJ-3EKF33R2V
R232, R233	2	L_RES 0603 51.1 Ohm 1/16W 1%	PAN	ERJ-3EKF51R1V
R119, R278, R280, R284, R286, R290, R292, R296, R298, R302, R304, R310, R312, R316, R318, R322, R324	17	L_RES 0603 1.0K Ohm 1/16W 5%	PAN	ERJ-3GEYJ102V
R10-R18, R118, R121- R132, R135-R138, R140-R142, R145, R279, R281, R285, R287, R291, R293, R297, R299, R303, R305, R306, R311, R313, R317, R319, R323, R325	47	L_RES 0603 10K Ohm 1/16W 5%	PAN	ERJ-3GEYJ103V

[查询"DS26519DK"供应商](#)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R139	1	RES 0603 1.0M Ohm 1/16W 5%	PAN	ERJ-3GEYJ105V
R21, R23, R25, R26, R28-R74, R224-R231, R328	60	L_RES 0603 33 Ohm 1/16W 5%	PAN	ERJ-3GEYJ330V
R1-R5, R116, R117, R282, R283, R288, R289, R294, R295, R300, R301, R307-R309, R314, R315, R320, R321, R326, R327	24	L_RES 0603 330 Ohm 1/16W 5%	PAN	ERJ-3GEYJ331V
R234	1	RES 0603 3.3K Ohm 1/16W 5%	PAN	ERJ-3GEYJ332V
R235, R236	2	RES 0603 4.7K Ohm 1/16W 5%	PAN	ERJ-3GEYJ472V
SW2	1	L_SWITCH MOM 4PIN SINGLE POLE	PAN	EVQPAE04M
J12	1	HEADER, 14 PIN, DUAL ROW, VERT	STC	HDR-TSW-107-14-T-D
J5-J11, J15-J23	16	HEADER, 20 PIN, DUAL ROW, VERT	STC	HDR-TSW-110-14-T-D
DS1, DS2	2	LED, RED, SMD	PAN	LN1251C
DS3-DS19	17	L_LED, RED, SMD	PAN	LN1251C
U3	1	L_IC, LINEAR REGULATOR, 1.5W, 1.8V OR ADJ, 1A, 16 PIN TSSOP-EP	MAX	MAX1793EUE-18
U4	1	IC, LINEAR REGULATOR, 1.5W, 2.5V OR ADJ, 1A, 16 PIN TSSOP-EP	MAX	MAX1793EUE-25
U9	1	IC, OPEN DRAIN MICROPROCESSOR RESET CKT, 3.08V 140MS, 4PIN SOT143	MAX	MAX6315US31D3-T
U10	1	MICROPROCESSOR RESET CIRCUITS, 3.08V RESET, 3 PIN SC70	MAX	MAX803TEXR-T
U8	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	MAX	MAX811TEUS-T
U5	1	IC, MCORE MICROCONTROLLER, 144 PIN LQFP	MOT	MMC2107PV
JMP7-JMP66, JMP71-JMP106	96	DO NOT PLACE, OPEN 2PIN TH JUMPER	NA	NA
R133, R147	2	RES 0603 DO NOT POPULATE	NA	NA
TP1-TP28, TP37-TP48, TP50	41	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U13-U16, U18-U34	21	L_TINYLOGIC HIGH SPEED 2-INPUT OR GATE, 5 PIN SOT23	FAI	NC7SZ32M5
J1	1	L_CONN, 12 PIN, DUAL ROW, VERT	SUL	PTC06DAAN
J24, J25	2	CONNECTOR, STACKED OCTAL JACK, 64- PIN, SHIELDED	MOL	SD-44520-001
U1	1	SOCKET, SURFACE MOUNT, BGA, 484P, 1MM	IRO	SG-BGA-6120
SW1	1	L_SWITCH, SPDT SLIDE, 3PIN TH	TYC	SSA12
JMP1-JMP6, JMP67, JMP69	8	L_2 PIN HEADER, .100 CENTERS, VERTICAL	STC	TSW-102-07-T-S
JMP68, JMP70	2	L_HEADER, 3-PIN, .100 CENTERS, VERTICAL	STC	TSW-103-07-T-S
J14	1	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	STC	TSW-105-07-T-D
T1-T4	4	XFMR, XMIT/RCV, 1 TO 2 AND 1 TO 1, SMT 32 PIN	PUL	TX1475

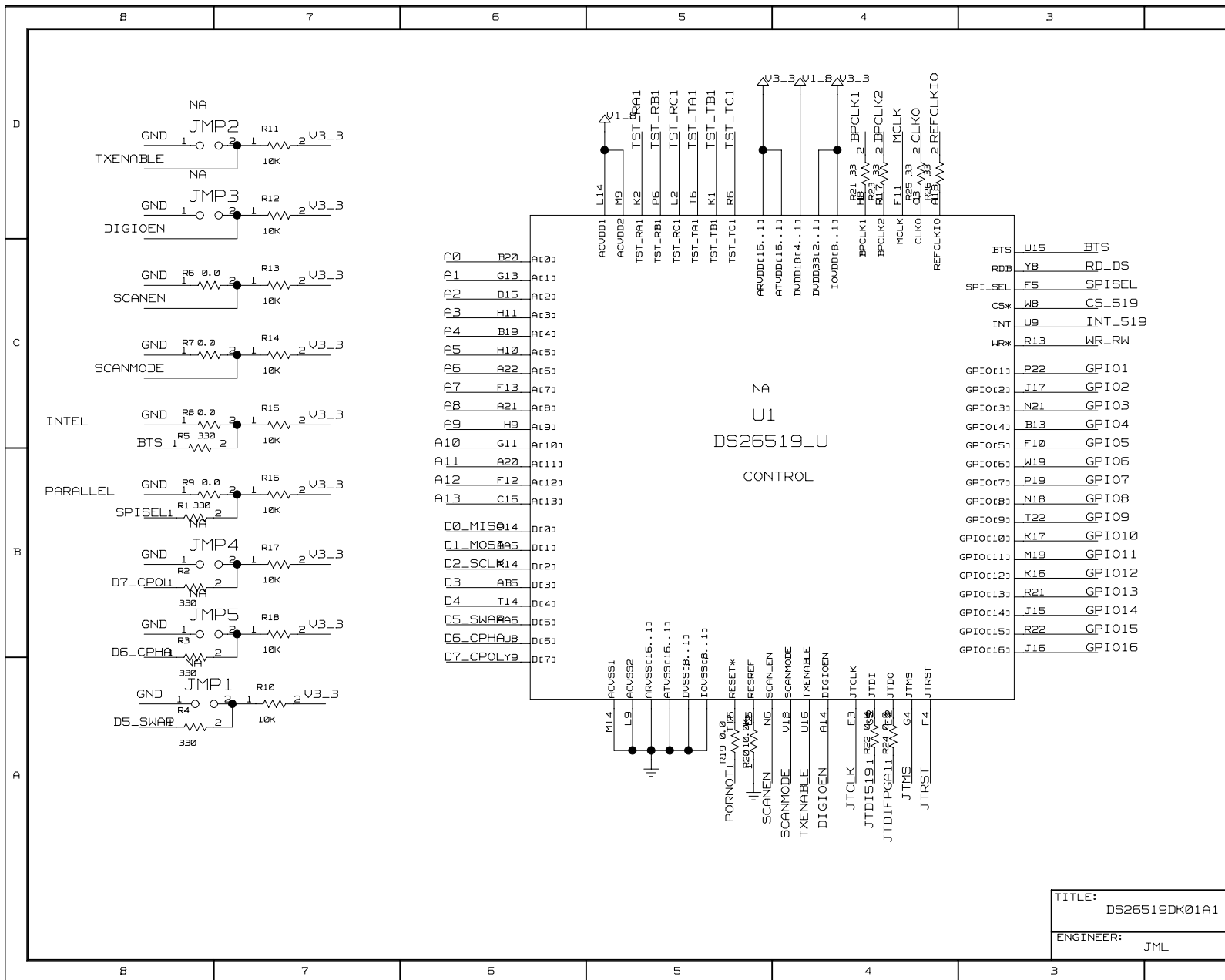
[查询"DS26519DK"供应商](#)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
L1	1	INDUCTOR 1.0uH 2PIN SMT 20%	COT	UP1B-1R0
U2, U12	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	XIL	XC2S50-5FG256C
U17	1	IC, PLATFORM FLASH IN-SYS PROG CONFIG PROM, 2MBIT, 20 PIN TSSOP	XIL	XCF02SVO20C

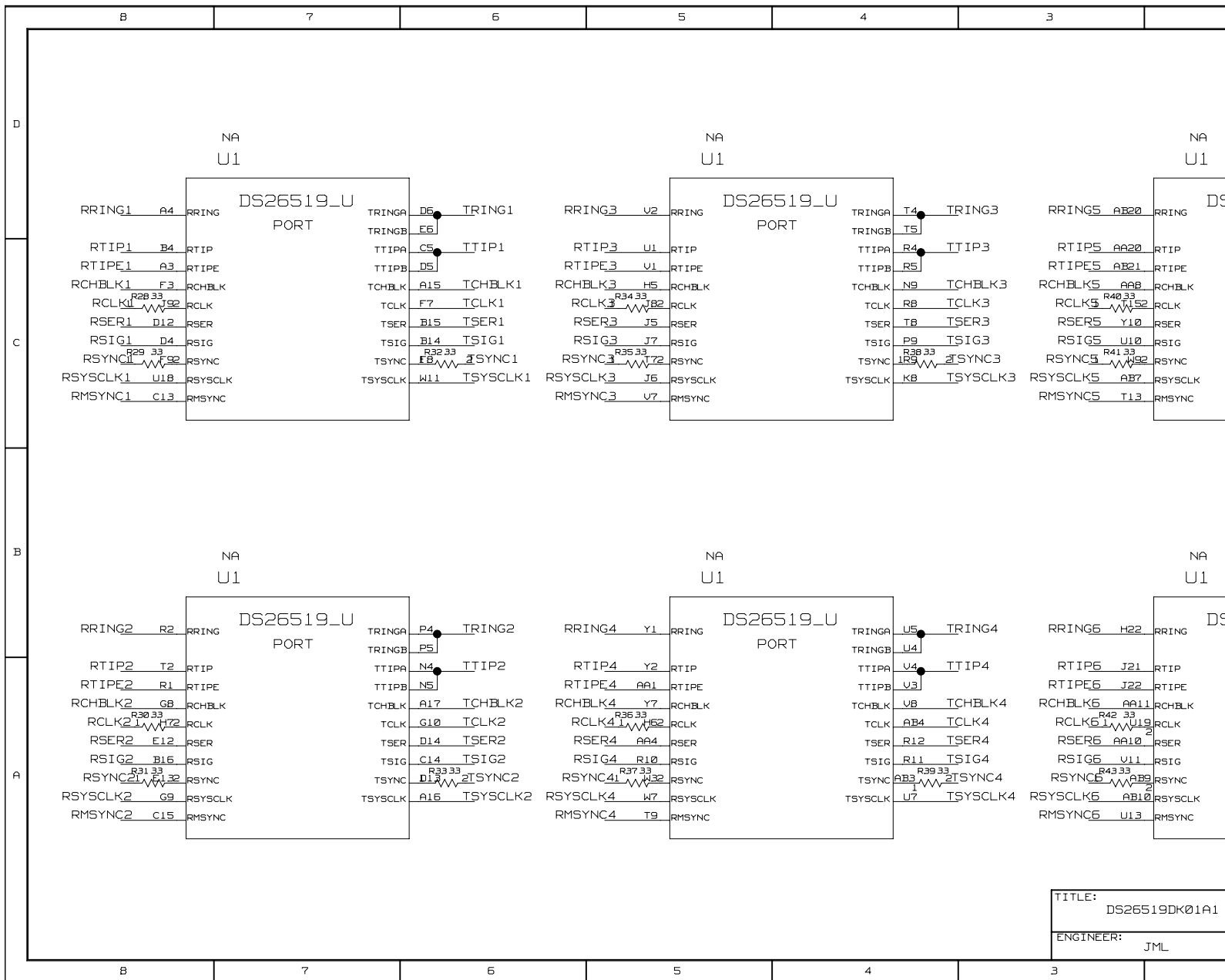
12. SCHEMATICS

The schematics are featured in the following pages.

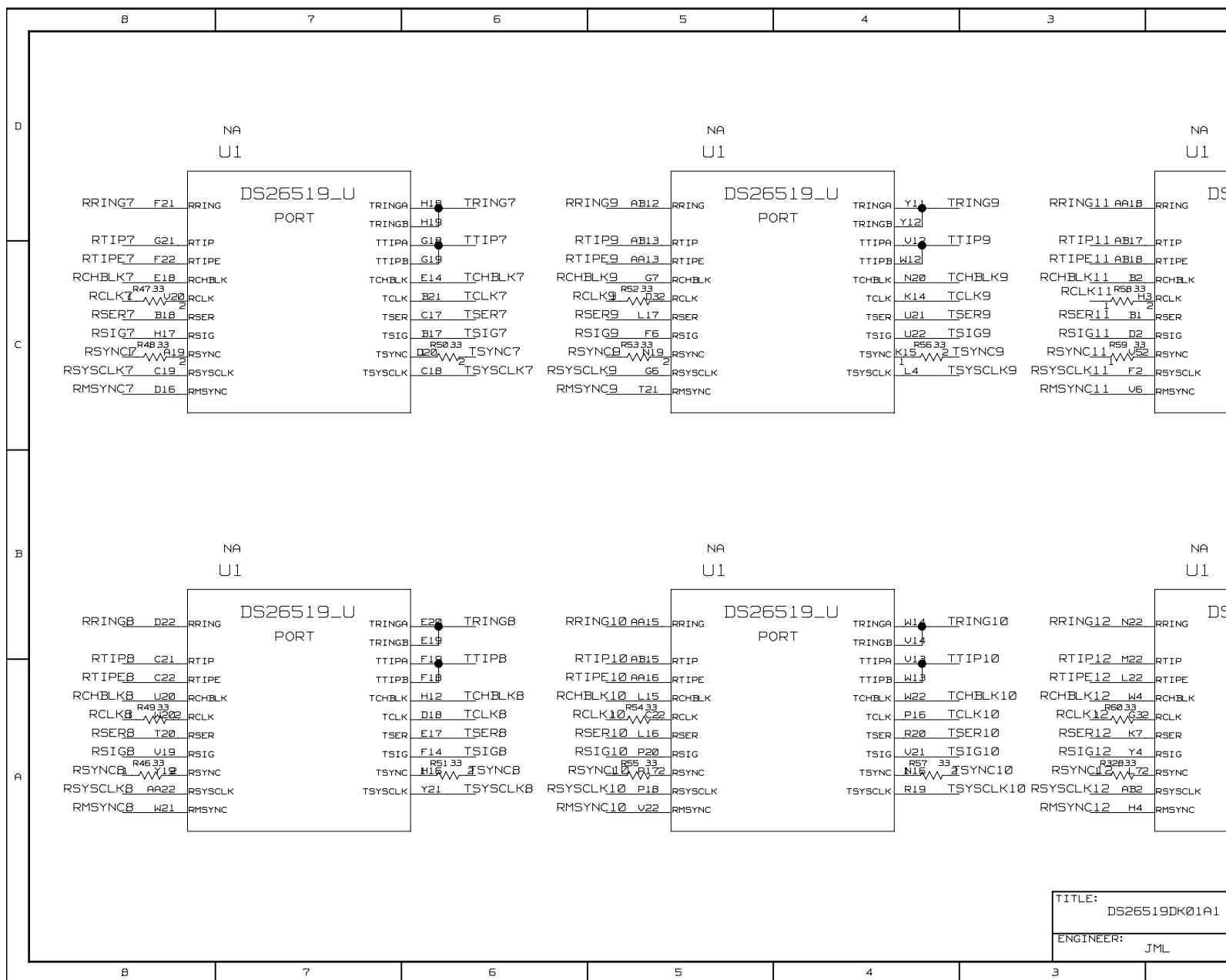
查询"DS26519DK"供应商



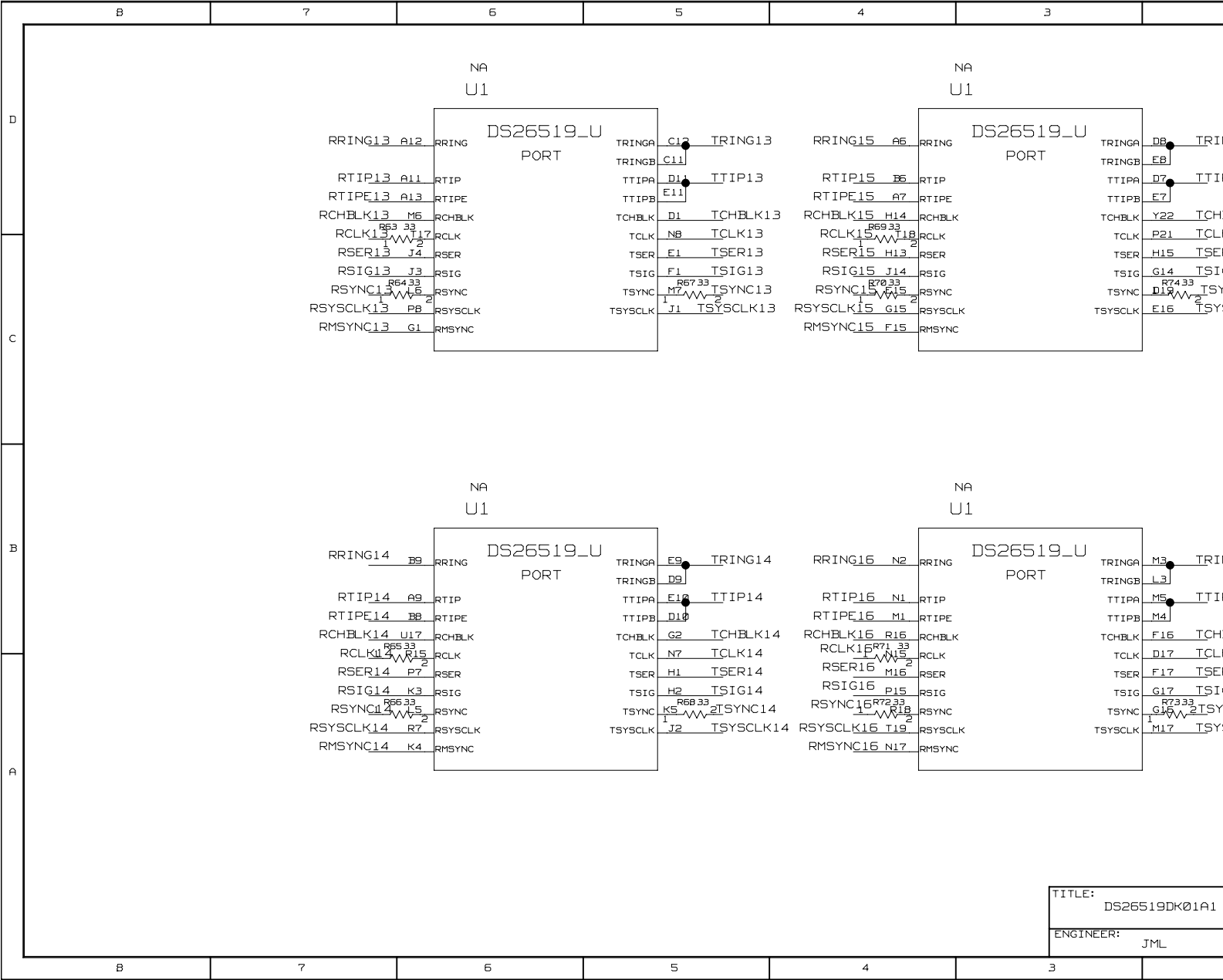
查询"DS26519DK"供应商



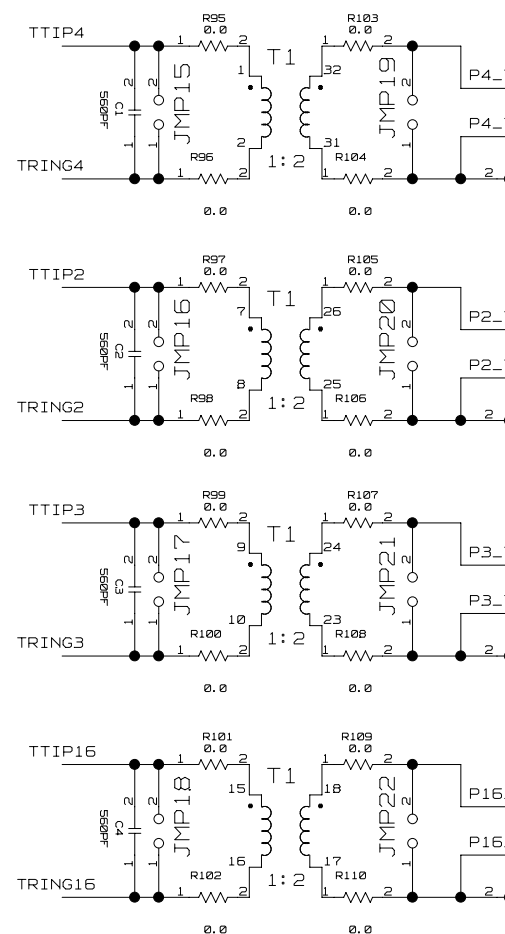
查询"DS26519DK"供应商



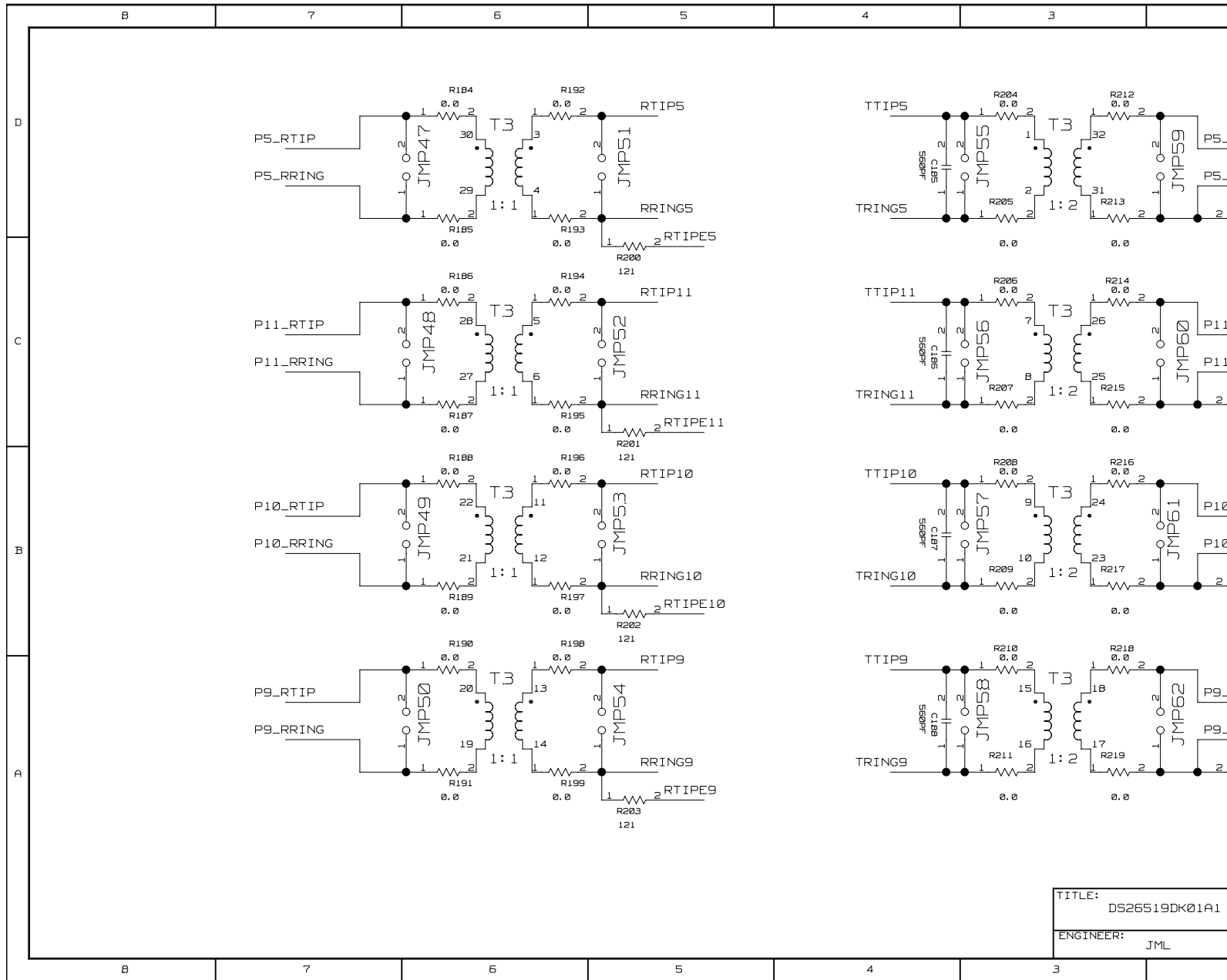
查询"DS26519DK"供应商

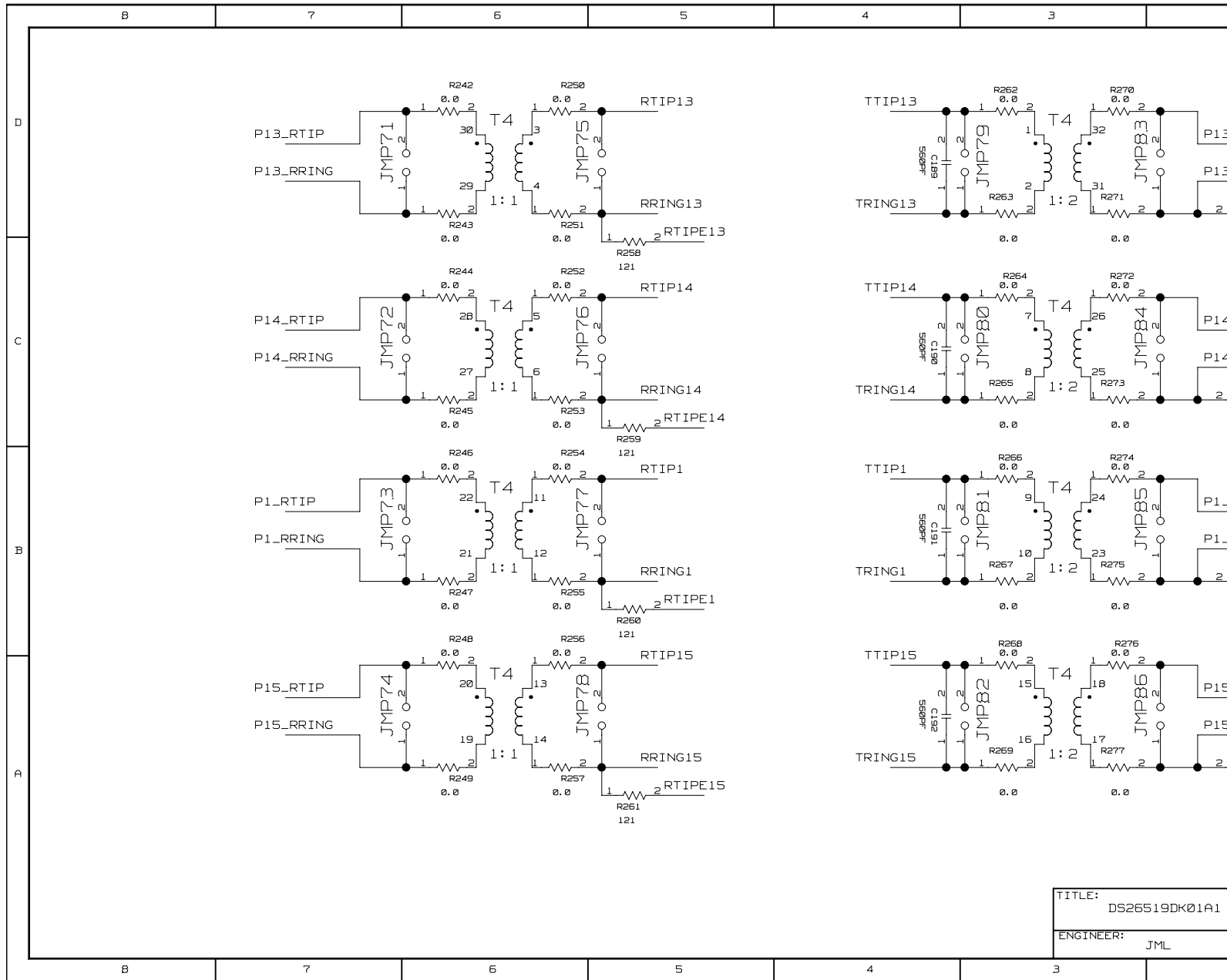


查询"DS26519DK"供应商

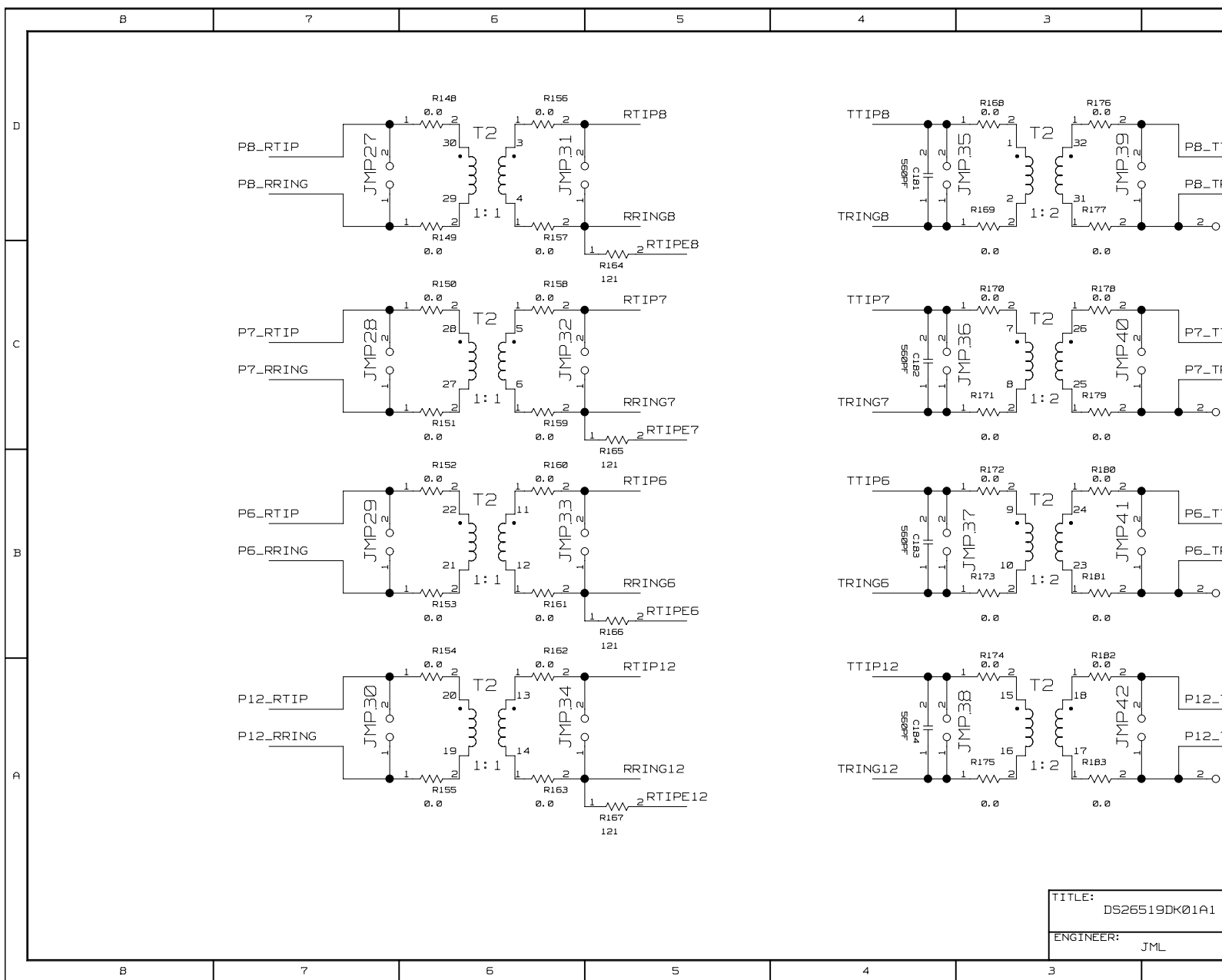


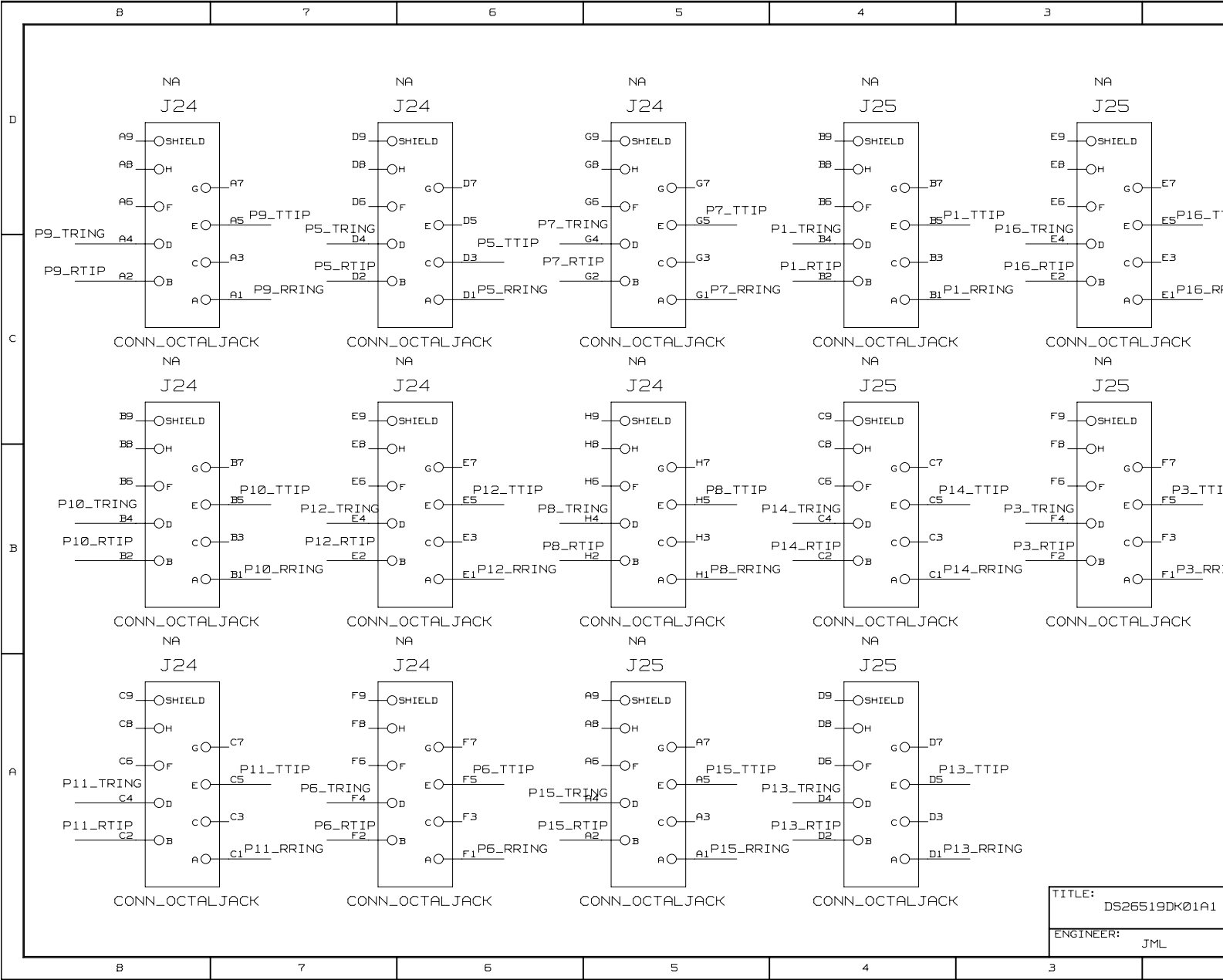
TITLE:	DS26519DK01
ENGINEER:	JML





查询"DS26519DK"供应商





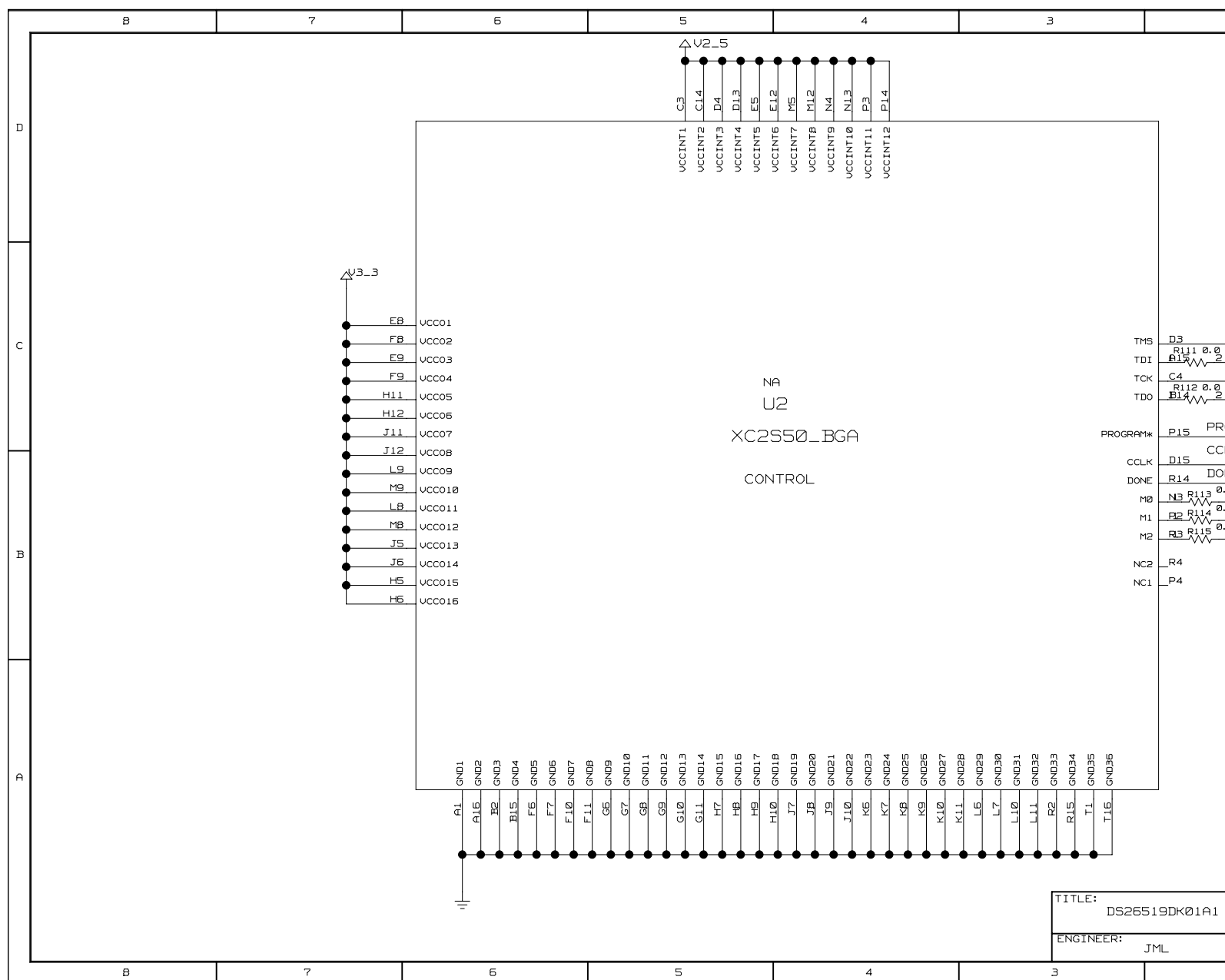
D		C		B		A		
B	7	6	5	4	3			
CLOCK1		BB	GCK3	BANK 1		I02_1\IRDY		
PD31	A7	I01_0	NA		I02_2\UREF		H16 D7_CPOL	
PD30	B7	I02_0\UREF	U2		I03_2\D3		H15 D6_CPHA	
PD29	C7	I03_0	XC2S50_BGA		I04_2		G16 D5_SWAP	
PD28	B6	I04_0	0 KINGI		I05_2		H13 D4	
PD27	A6	I05_0	BANK 2		I06_2\D2		G13 D3	
PD26	C6	I06_0	I012_2\<DIN, D0>		I07_2\D1		F15 D2_SCLK	
PD25	B4	I07_0\UREF	I013_2\<DOUT, BUSY>		I08_2		E16 D1_MOSI	
PD24	A3	I08_0	I014_2		I09_2		F14 D0_MISO	
PA14	B3	I09_0	I015_2		I010_2\UREF		D16 A12	
PA13	DB	I010_0	I011_2		I011_2		F13 A11	
PA12	A6	I011_0	I012_2\<DIN, D0>		I011_2		E13 A10	
PA11	CB	I012_0	I013_2\<DOUT, BUSY>		I012_2\<DIN, D0>		D14 FPGA1_DIN	
PA10	D7	I013_0	I014_2		I013_2\<DOUT, BUSY>		C15 FPGA2_DIN	
PA9	E7	I014_0	I015_2		I014_2		H14 A8	
PA8	B6	I015_0	I016_2		I015_2		J13 A7	
PA7	D6	I016_0	I017_2		I016_2		G14 A6	
PA6	A4	I017_0	I018_2		I017_2		G15 A5	
PA5	E6	I018_0	I019_2		I018_2		G12 A4	
PA4	D5	I019_0	I020_2		I019_2		F16 A3	
PA3	C5	I020_0	I021_2		I020_2		F12 A2	
FPGA_INIT		N15	I01_3\INIT*	BANK 3		I021_2		E15 A1
PA2	N14	I02_3\ND7	I012_3		I022_2		E14 A0	
PA1	M13	I03_3	I013_3		I023_2		C16 A13	
PA0	L14	I04_3\UREF	I014_3		I024_2		B16 A14	
INT_519	P16	I05_3	I015_3		I016_3			
PA15	L13	I06_3	I017_3\ND6		I017_3			
2d11	I	N16	I018_3\ND5		I018_3			
Ed1	I	M16	I019_3		I019_3			
4d11	I	K14	I010_3\UREF		I020_3			
5d11	I	K16	I011_3\ND4		I021_3			
9d11	I	J16	I012_3		I022_3			
CLROUT	K15	I012_3	I013_3\IRDY		I023_3			
MOSI	J15	I014_3	I014_3		I024_3			
MISO	T15	I015_3	I015_3		I025_3			
SS	R16	I016_3	I016_3		I026_3			
ONCE_RESET	M14	I017_3	I017_3		I027_3			
PORNOT	L12	I018_3	I018_3		I028_3			
CS_1SEL	L16	I019_3	I019_3		I029_3			
BTS	L15	I020_3	I020_3		I030_3			
WR_RW	K12	I021_3	I021_3		I031_3			
RD_DS	J14	I022_3	I022_3		I032_3			
GCK2		C9	OSC1_1544	BANK 1		I02_1\IRDY		
I01_1\CS*		B13	I01_1\CS*	NA		I02_2\UREF		
I02_1\WRITE*		C13	I02_1\WRITE*	U2		I03_2\D3		
I03_1		A14	I03_1	XC2S50_BGA		I04_2		
I04_1\UREF		C11	I04_1\UREF	0 KINGI		I05_2		
I05_1		E11	I05_1	BANK 2		I06_2\D2		
I06_1		B11	I06_1	I012_2\<DIN, D0>		I07_2\D1		
I07_1		A11	I07_1	I013_2\<DOUT, BUSY>		I08_2		
I08_1		C10	I08_1	I014_2		I09_2		
I09_1\UREF		B9	I09_1\UREF	I015_2		I010_2\UREF		
I010_1		D9	I010_1	I011_2		I011_2		
I011_1		A8	I011_1	I012_2\<DIN, D0>		I011_2		
I012_1		C12	I012_1	I013_2\<DOUT, BUSY>		I012_2\<DIN, D0>		
I013_1		D12	I013_1	I014_2		I013_2\<DOUT, BUSY>		
I014_1		B12	I014_1	I015_2		I014_2		
I015_1		A13	I015_1	I016_2		I015_2		
I016_1		D11	I016_1	I017_2		I016_2		
I017_1		A12	I017_1	I018_2		I017_2		
I018_1		B10	I018_1	I019_2		I018_2		
I019_1		D10	I019_1	I020_2		I019_2		
I020_1		A10	I020_1	I021_2		I020_2		
I021_1		E10	I021_1	I022_2		I021_2		
I022_1		A9	I022_1	I023_2		I022_2		
GCK3		B8	GCK3	BANK 3		I023_2		
I01_1\CS*		B13	I01_1\CS*	NA		I024_2		
I02_1\WRITE*		C13	I02_1\WRITE*	U2		I025_2		
I03_1		A14	I03_1	XC2S50_BGA		I026_2		
I04_1\UREF		C11	I04_1\UREF	0 KINGI		I027_2		
I05_1		E11	I05_1	BANK 2		I028_2		

TITLE: DS26519DK01A1

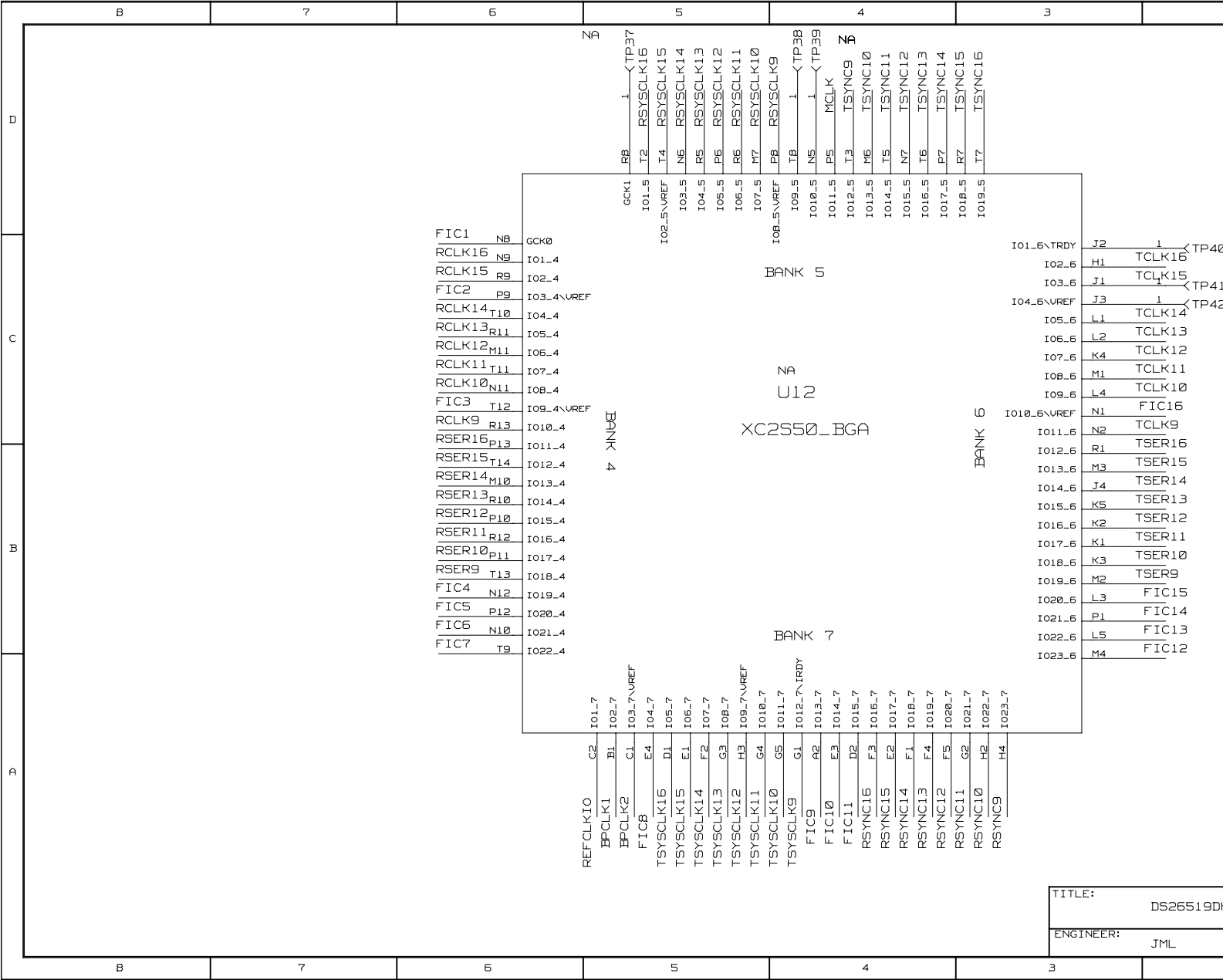
ENGINEER: JML

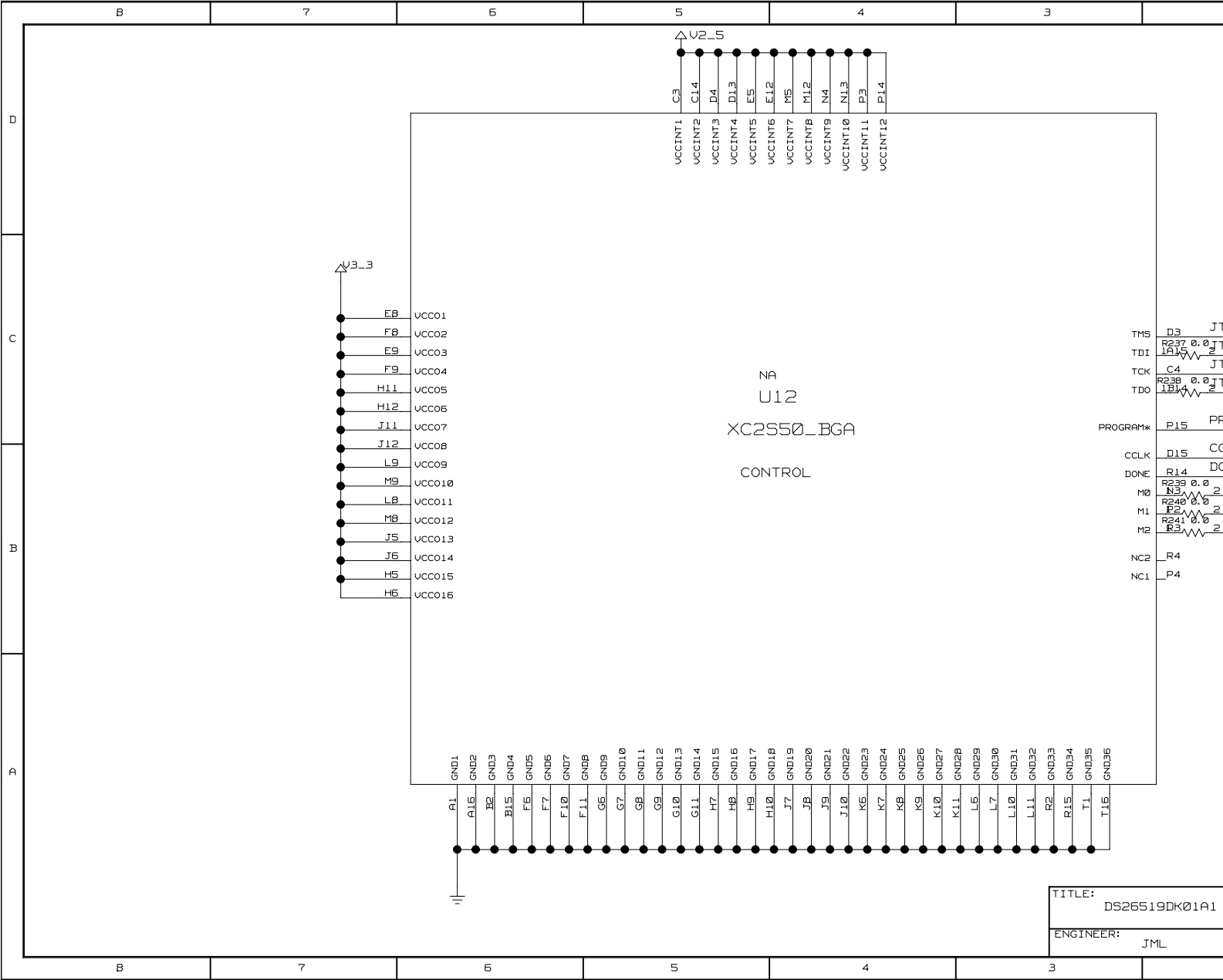
D		C		B		A	
B		7		6		5	
7		6		5		4	
6		5		4		3	
5		4		3		2	
4		3		2		1	
3		2		1			
2		1					
1							

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D		B	7	6	5	4	3	
C	B	D	C	B	D	C	B	D
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D	C	B	D	C
B	D	C	B	D				





	B	7	6	5	4	3		
D		NA J15 RCLK11 TCLK13 RSER15 TSER17 RSYNC19 TSYNC111 RCHBLK113 TCHBLK115 RSYSCLK117 TSYSCLK119 12 34 56 78 910 1112 1314 1516 1718 1920 GND GND GND GPIO1 RMSYNC1 RSIG1 TSIG1 GND GND NA J16 RCLK21 TCLK23 RSER25 TSER27 RSYNC29 TSYNC211 RCHBLK213 TCHBLK215 RSYSCLK217 TSYSCLK219 12 34 56 78 910 1112 1314 1516 1718 1920 GND GND GND GPIO2 RMSYNC2 RSIG2 TSIG2 GND GND GND NA J17 RCLK31 TCLK33 RSER35 TSER37 RSYNC39 TSYNC311 RCHBLK313 TCHBLK315 RSYSCLK317 TSYSCLK319 12 34 56 78 910 1112 1314 1516 1718 1920 GND GND GND GPIO3 RMSYNC3 RSIG3 TSIG3 GND GND GND						
C		NA J18 RCLK41 TCLK43 RSER45 TSER47 RSYNC49 TSYNC411 RCHBLK413 TCHBLK415 RSYSCLK417 TSYSCLK419 12 34 56 78 910 1112 1314 1516 1718 1920 GND GND GND GPIO4 RMSYNC4 RSIG4 TSIG4 GND GND GND NA J19 RCLK51 TCLK53 RSER55 TSER57 RSYNC59 TSYNC511 RCHBLK513 TCHBLK515 RSYSCLK517 TSYSCLK519 12 34 56 78 910 1112 1314 1516 1718 1920 GND GND GND GPIO5 RMSYNC5 RSIG5 TSIG5 GND GND GND NA J20 RCLK61 TCLK63 RSER65 TSER67 RSYNC69 TSYNC611 RCHBLK613 TCHBLK615 RSYSCLK617 TSYSCLK619 12 34 56 78 910 1112 1314 1516 1718 1920 GND GND GND GPIO6 RMSYNC6 RSIG6 TSIG6 GND GND GND						
B								
A								
	SYSTEM CONNECTORS						TITLE: DS26519DK01A1 ENGINEER: JML	
	B	7	6	5	4	3		

NA
J18

RCLK41

TCLK43

RSER45

TSER47

RSYNC49

TSYNC411

RCHBLK413

TCHBLK415

RSYSCLK417

TSYSCLK419

12

34

56

78

910

1112

1314

1516

1718

1920

GND

GND

GND

GPIO4

RMSYNC4

RSIG4

TSIG4

GND

GND

GND

NA
J19

RCLK51

TCLK53

RSER55

TSER57

RSYNC59

TSYNC511

RCHBLK513

TCHBLK515

RSYSCLK517

TSYSCLK519

12

34

56

78

910

1112

1314

1516

1718

1920

GND

GND

GND

GPIO5

RMSYNC5

RSIG5

TSIG5

GND

GND

GND

NA
J20

RCLK61

TCLK63

RSER65

TSER67

RSYNC69

TSYNC611

RCHBLK613

TCHBLK615

RSYSCLK617

TSYSCLK619

12

34

56

78

910

1112

1314

1516

1718

1920

GND

GND

GND

GPIO6

RMSYNC6

RSIG6

TSIG6

GND

GND

GND

NA
J21

RCLK71

TCLK73

RSER75

TSER77

RSYNC79

TSYNC711

RCHBLK713

TCHBLK715

RSYSCLK717

TSYSCLK719

12

34

56

78

910

1112

1314

1516

1718

1920

GND

GND

GND

GPIO7

RMSYNC7

RSIG7

TSIG7

GND

GND

GND

CONN_20P

CONN_20P

CONN_20P

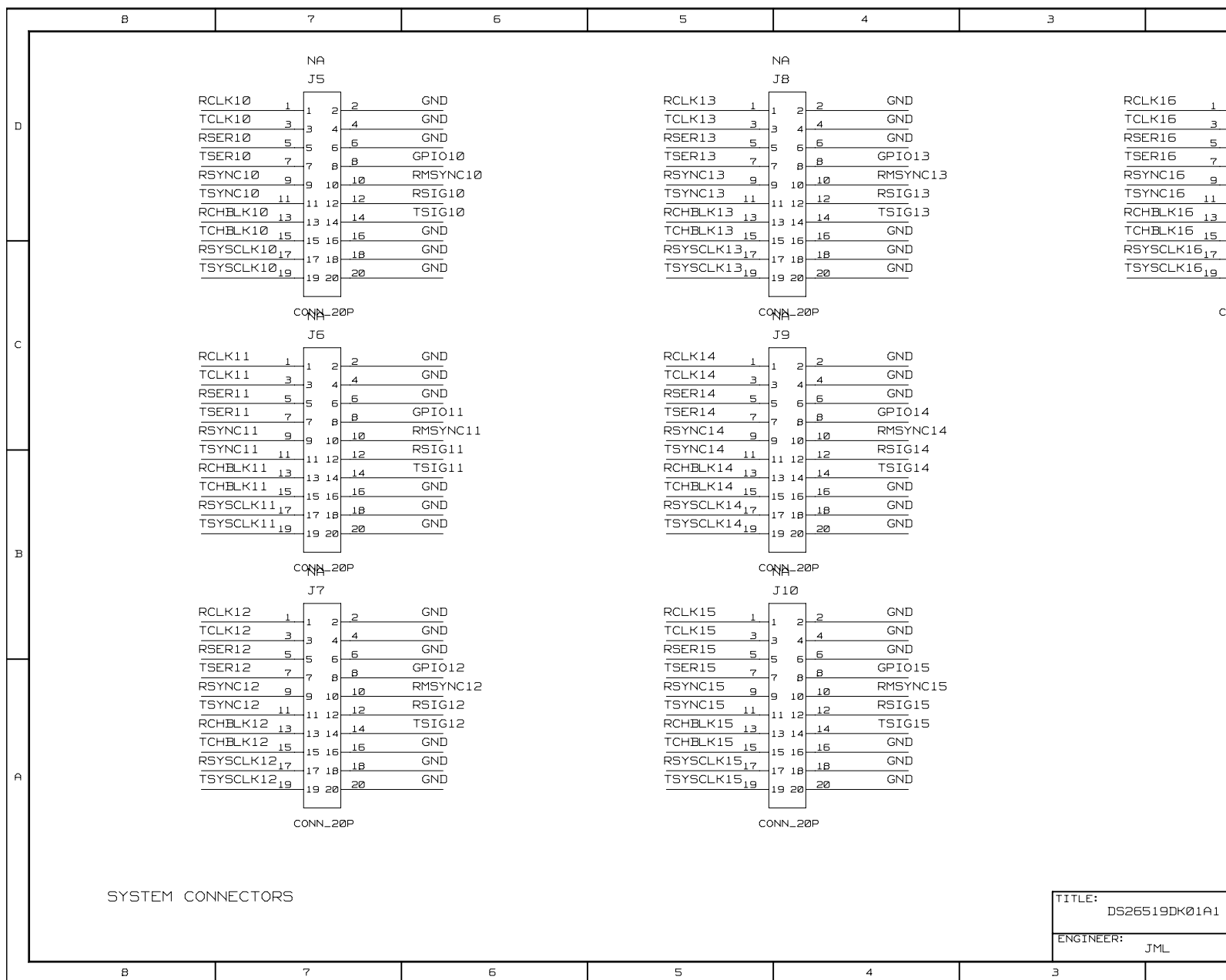
CONN_20P

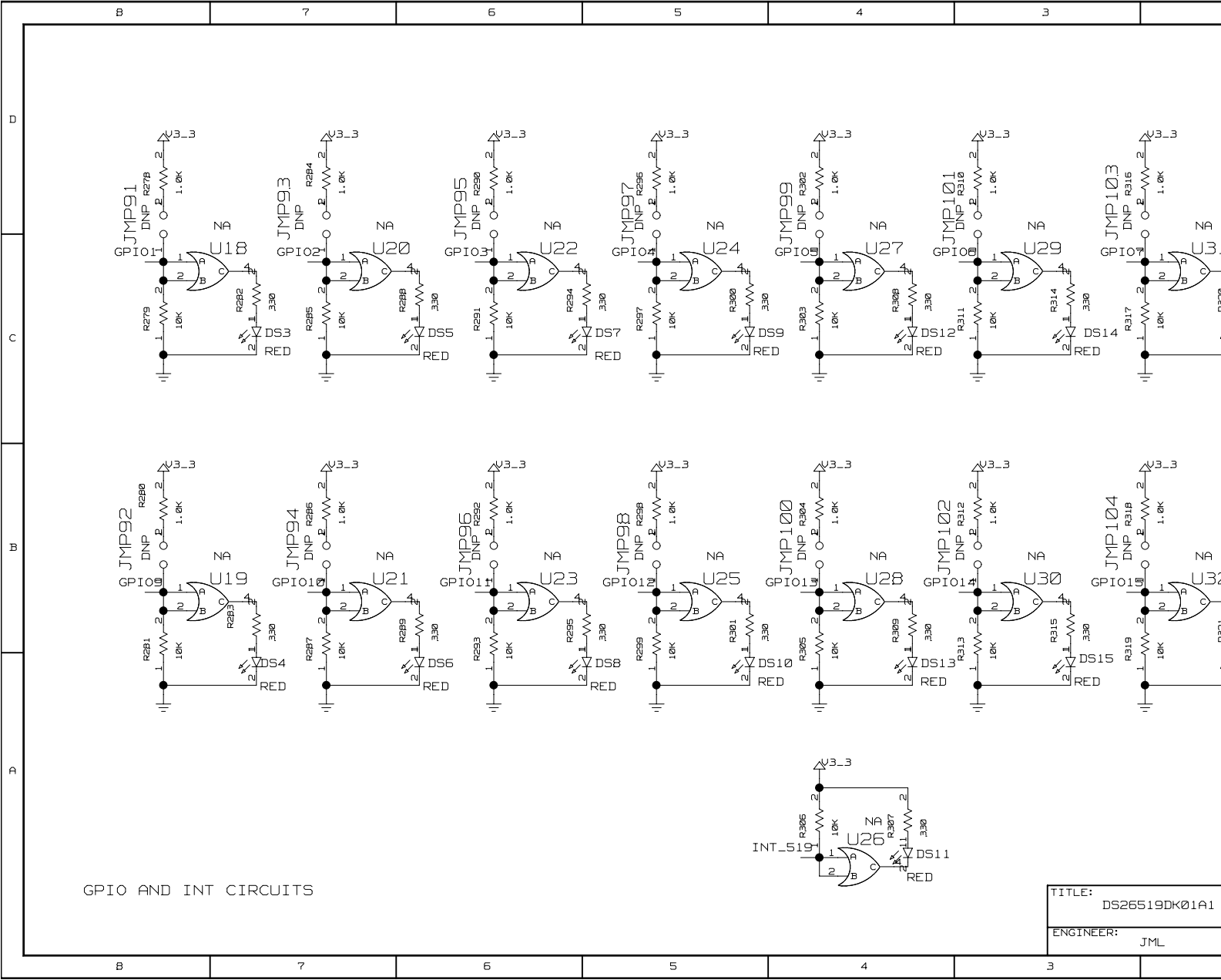
CONN_20P

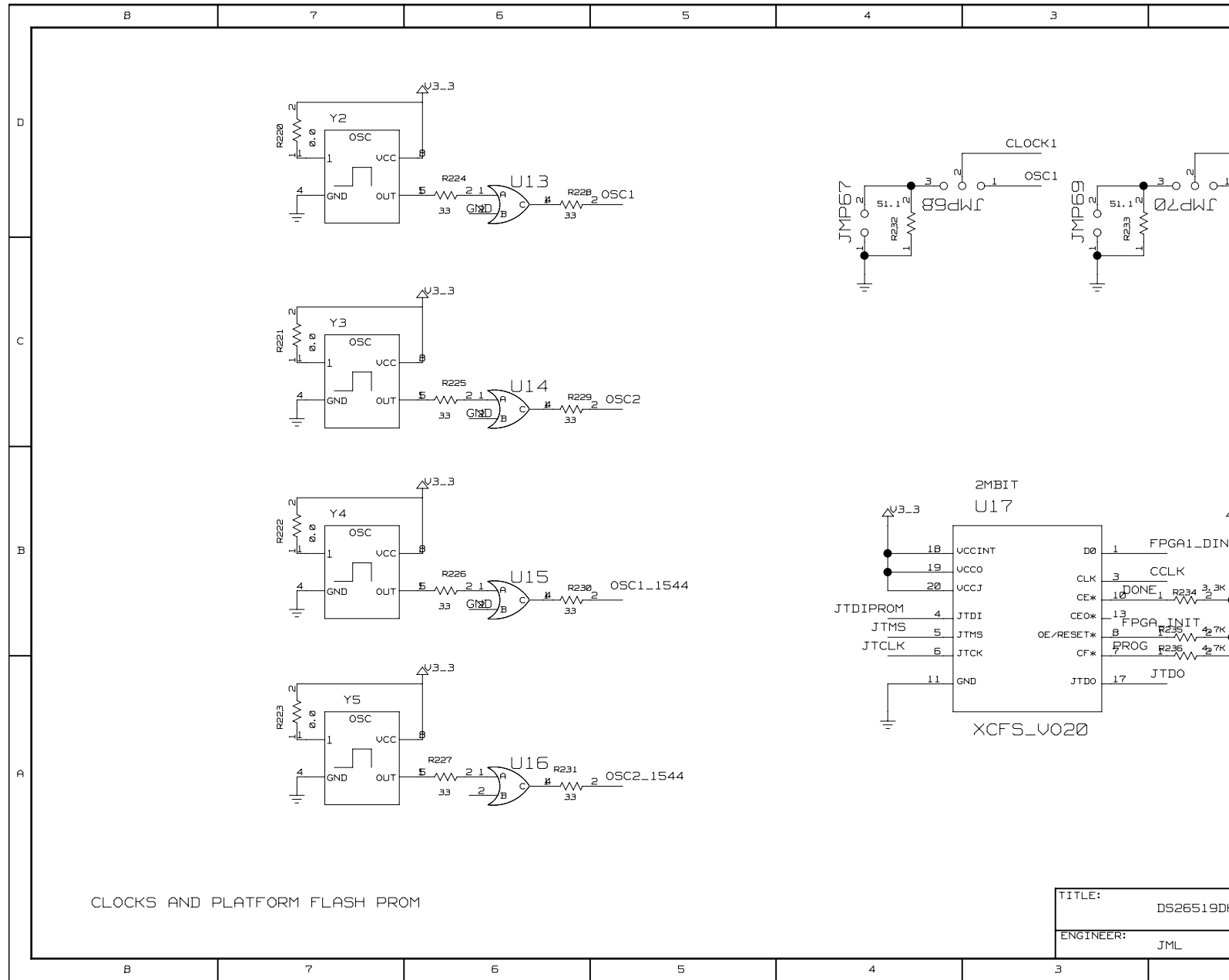
CONN_20P

CONN_20P

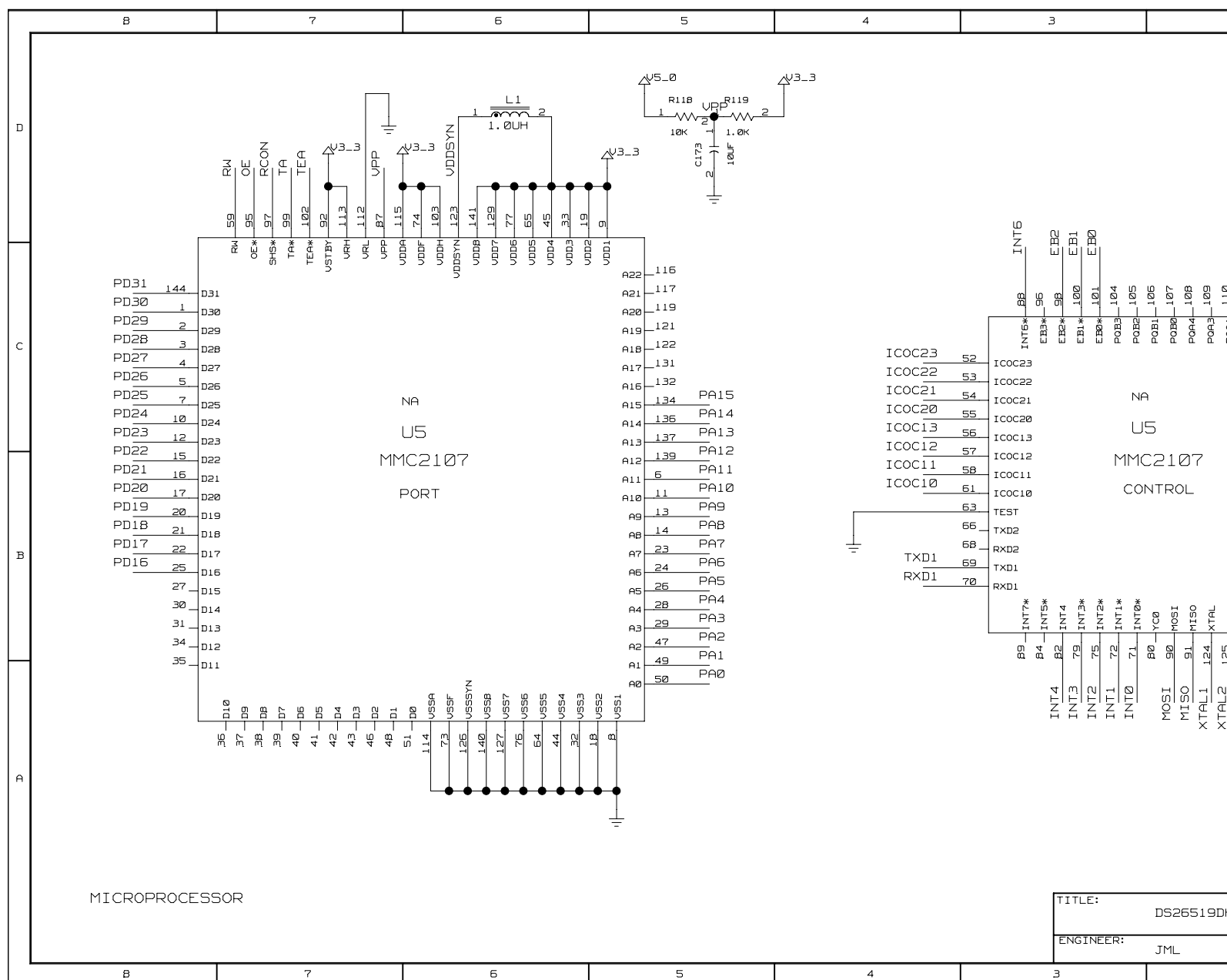
查询"DS26519DK"供应商

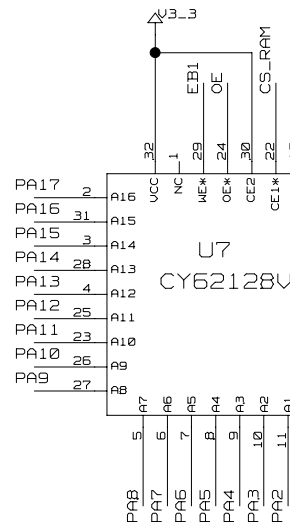
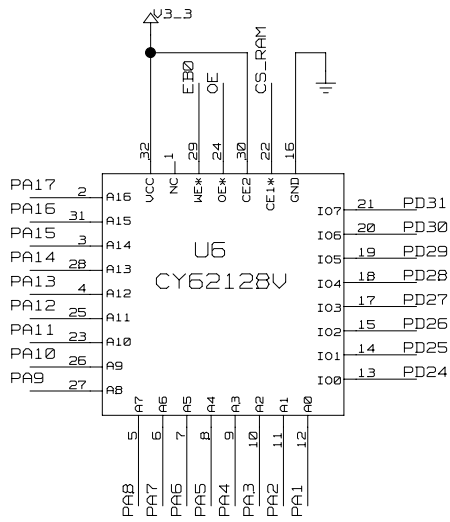






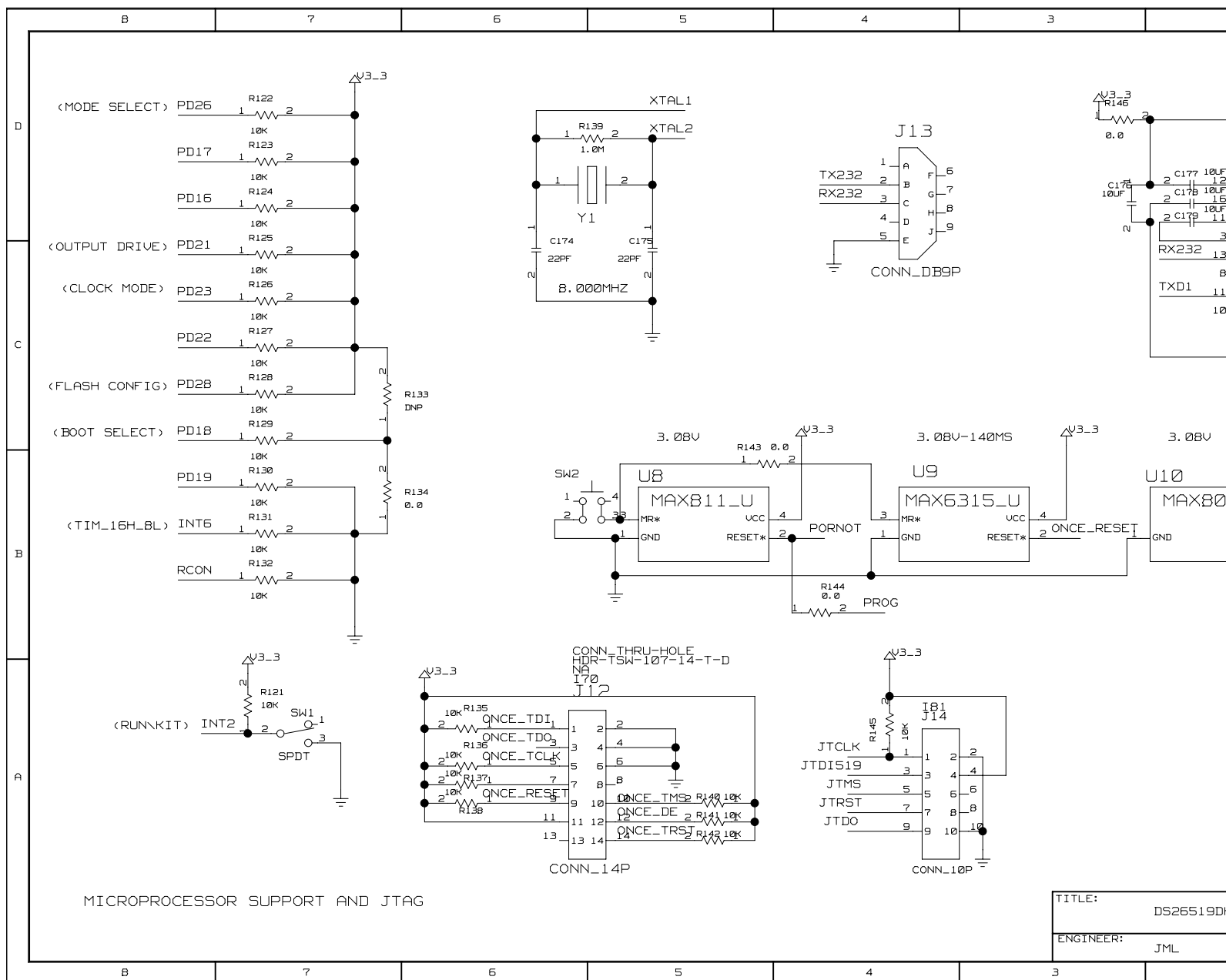
查询"DS26519DK"供应商

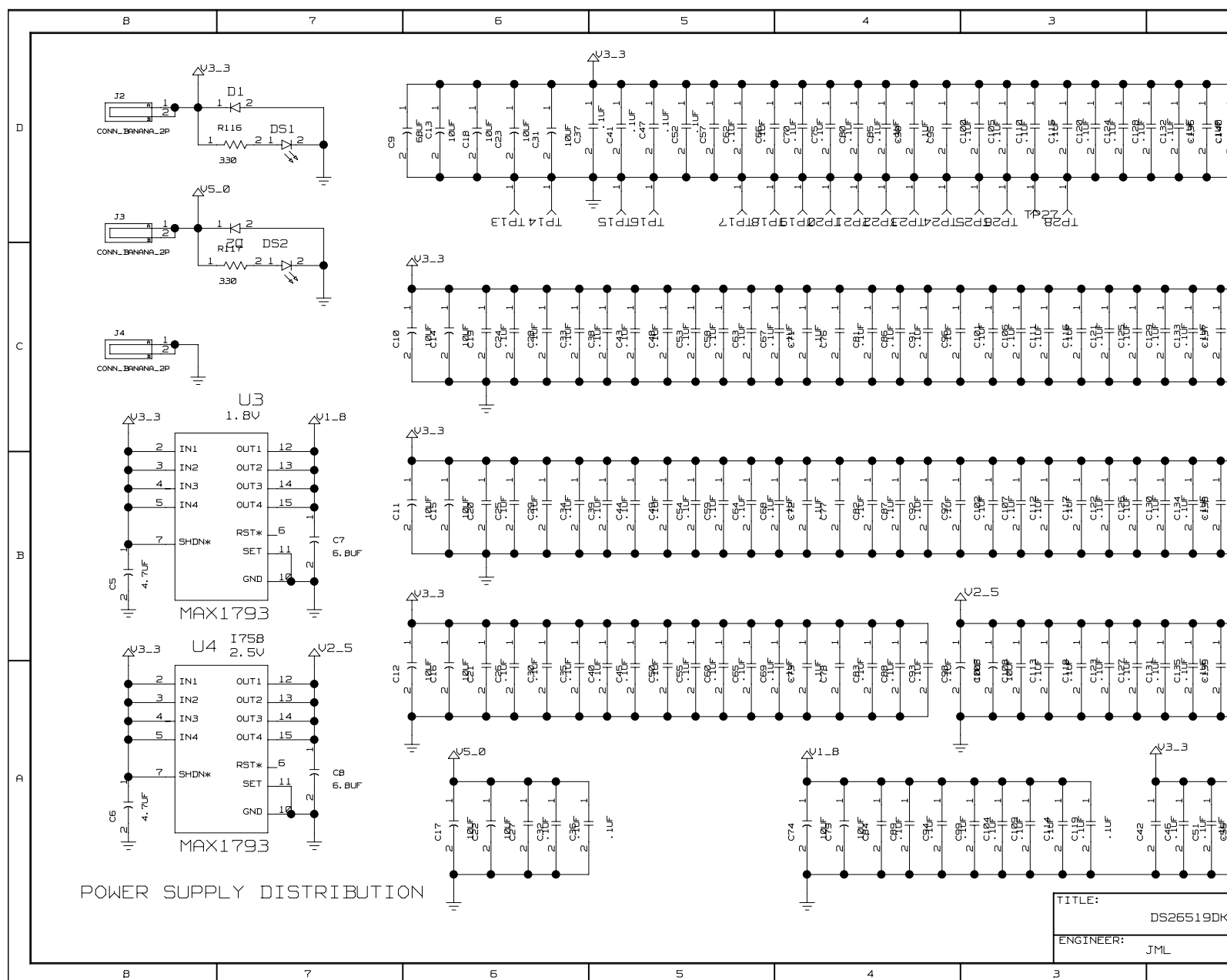




MICROPROCESSOR MEMORY

TITLE: DS26519DK
ENGINEER: JML





	B	7	6	5	4	3	
D	REVISION HISTORY - 070606 - 01 - INITIAL RELEASE FOR DESIGN REVIEW 080906 - A0 - RELEASE FOR FAB QUOTES 012507 - A1 - MODE PINS AND INT PINS FOR FPGA PINOUT ON 8-PORT RJ48 CONNECTORS						
C							
B							
A							
	B	7	6	5	4	3	
							TITLE:DS26519DK ENGINEER:JML