

查询"5962-89946012X"供应商

[illegible]

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SEP 87

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5962-E1682

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89946	01	E	X
┆	┆	┆	┆
┆	┆	┆	┆
┆	┆	┆	┆
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC190	4-bit synchronous, decade up/down counter

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal .358" x .358" x .100"), leadless chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range - - - - -	-0.5 V dc to +7.0 V dc
DC input voltage range - - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range - - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
Clamp diode current - - - - -	±20 mA
DC output current (per pin) - - - - -	±25 mA
DC V_{CC} or GND current (per pin) - - - - -	±50 mA
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation (P_D) 2/ - - - - -	500 mW
Lead temperature (soldering, 10 seconds) - - - - -	+260°C
Thermal resistance, junction-to-case (θ_{JC}) - - - - -	See MIL-M-38510, appendix C
Junction temperature (T_J) - - - - -	+175°C

1.4 Recommended operating conditions.

Supply voltage range - - - - -	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN}) - - - - -	0.0 V to V_{CC}
Output voltage range (V_{OUT}) - - - - -	0.0 V to V_{CC}
Case operating temperature range (T_C) - - - - -	-55°C to +125°C
Input rise or fall time:	
$T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$:	
$V_{CC} = 2.0$ V - - - - -	0 to 500 ns
$V_{CC} = 4.5$ V - - - - -	0 to 500 ns
$V_{CC} = 6.0$ V - - - - -	0 to 400 ns

1/ Unless otherwise specified, all voltages are referenced to ground.

2/ For $T_C = +100^\circ\text{C}$ to $+125^\circ\text{C}$, derate linearly at 12 mW/°C.

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Minimum pulse width, CP (t_{w1}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	125 ns
$V_{CC} = 4.5\text{ V dc}$	25 ns
$V_{CC} = 6.0\text{ V dc}$	21 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	190 ns
$V_{CC} = 4.5\text{ V dc}$	38 ns
$V_{CC} = 6.0\text{ V dc}$	32 ns

Minimum pulse width, $\overline{\text{LOAD}}$ (t_{w2}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	120 ns
$V_{CC} = 4.5\text{ V dc}$	24 ns
$V_{CC} = 6.0\text{ V dc}$	20 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	180 ns
$V_{CC} = 4.5\text{ V dc}$	36 ns
$V_{CC} = 6.0\text{ V dc}$	31 ns

Minimum setup time, Dn to $\overline{\text{LOAD}}$ (t_{s1}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	150 ns
$V_{CC} = 4.5\text{ V dc}$	30 ns
$V_{CC} = 6.0\text{ V dc}$	25 ns
$T_C = -55^\circ\text{C to } +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	225 ns
$V_{CC} = 4.5\text{ V dc}$	45 ns
$V_{CC} = 6.0\text{ V dc}$	38 ns

Maximum operating frequency (f_{max}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	4.2 MHz
$V_{CC} = 4.5\text{ V dc}$	21 MHz
$V_{CC} = 6.0\text{ V dc}$	24 MHz
$T_C = -55^\circ\text{C to } +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	2.8 MHz
$V_{CC} = 4.5\text{ V dc}$	14 MHz
$V_{CC} = 6.0\text{ V dc}$	16 MHz

Minimum setup time, Down/ $\overline{\text{Up}}$ to CLK (t_{s2}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	205 ns
$V_{CC} = 4.5\text{ V dc}$	41 ns
$V_{CC} = 6.0\text{ V dc}$	35 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	306 ns
$V_{CC} = 4.5\text{ V dc}$	61 ns
$V_{CC} = 6.0\text{ V dc}$	53 ns

Minimum setup time, $\overline{\text{Enable}}$ to CLK (t_{s3}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	205 ns
$V_{CC} = 4.5\text{ V dc}$	41 ns
$V_{CC} = 6.0\text{ V dc}$	35 ns
$T_C = -55^\circ\text{C to } +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	306 ns
$V_{CC} = 4.5\text{ V dc}$	61 ns
$V_{CC} = 6.0\text{ V dc}$	53 ns

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Minimum recovery time $\overline{LOAD}$ from CLK (t_{rec}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	150 ns
$V_{CC} = 4.5\text{ V dc}$	30 ns
$V_{CC} = 6.0\text{ V dc}$	25 ns
$T_C = -55^\circ\text{C to } +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	225 ns
$V_{CC} = 4.5\text{ V dc}$	45 ns
$V_{CC} = 6.0\text{ V dc}$	38 ns

Minimum hold time, Dn to $\overline{LOAD}$ (t_{h1}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	25 ns
$V_{CC} = 4.5\text{ V dc}$	5 ns
$V_{CC} = 6.0\text{ V dc}$	5 ns
$T_C = -55^\circ\text{C to } +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	40 ns
$V_{CC} = 4.5\text{ V dc}$	8 ns
$V_{CC} = 6.0\text{ V dc}$	7 ns

Minimum hold time, $\overline{Enable}$ to CLK (t_{h2}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	5 ns
$V_{CC} = 4.5\text{ V dc}$	5 ns
$V_{CC} = 6.0\text{ V dc}$	5 ns
$T_C = -55^\circ\text{C, } +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	5 ns
$V_{CC} = 4.5\text{ V dc}$	5 ns
$V_{CC} = 6.0\text{ V dc}$	5 ns

Minimum hold time, Down/ $\overline{Up}$ to CLK (t_{h3}):

$T_C = +25^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	5 ns
$V_{CC} = 4.5\text{ V dc}$	5 ns
$V_{CC} = 6.0\text{ V dc}$	5 ns
$T_C = -55^\circ\text{C to } +125^\circ\text{C}$:	
$V_{CC} = 2.0\text{ V dc}$	5 ns
$V_{CC} = 4.5\text{ V dc}$	5 ns
$V_{CC} = 6.0\text{ V dc}$	5 ns

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The functional diagram shall be as specified on figure 3.

3.2.4 Counting sequence. The counting sequence diagram shall be as specified on figure 4.

3.2.5 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

TABLE I. Electrical performance characteristics.							
Test	Symbol	Conditions -55°C < T _C < +125°C ^{1/} unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{IN} = V _{IH} minimum or V _{IL} maximum I _O ≤ 20 μA	V _{CC} = 2.0 V	1, 2, 3	1.9		V
			V _{CC} = 4.5 V		4.4		
			V _{CC} = 6.0 V		5.9		
		V _{IN} = V _{IH} minimum or V _{IL} maximum I _O ≤ 4.0 mA	V _{CC} = 4.5 V		3.7		
			V _{CC} = 6.0 V		5.2		
Low level output voltage	V _{OL}	V _{IN} = V _{IH} minimum or V _{IL} maximum I _O ≤ 20 μA	V _{CC} = 2.0 V	1, 2, 3		0.1	V
			V _{CC} = 4.5 V			0.1	
			V _{CC} = 6.0 V			0.1	
		V _{IN} = V _{IH} minimum or V _{IL} maximum I _O ≤ 4.0 mA	V _{CC} = 4.5 V			0.4	
			V _{CC} = 6.0 V			0.4	
High level input voltage ^{2/}	V _{IH}		V _{CC} = 2.0 V	1, 2, 3	1.5		V
			V _{CC} = 4.5 V		3.15		
			V _{CC} = 6.0 V		4.2		
See footnotes at end of table.							
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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Low level input voltage <u>2/</u>	V _{IL}		1, 2, 3		0.3	V
					0.9	
					1.2	
Quiescent supply current (standby)	I _{CC}	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	V _{CC} = 6.0 V	1, 2, 3	160	μA
Input leakage current	I _{IN}	V _{CC} = 6.0 V V _{IN} = V _{CC} or GND		1, 2, 3	±1.0	μA
Functional tests		See 4.3.1d	7, 8			
Propagation delay time, Enable to RC <u>3/</u>	t _{PHL1} , t _{PLH1}	T _C = +25°C C _L = 50 pF See figure 5	V _{CC} = 2.0 V	9	132	ns
			V _{CC} = 4.5 V		26	
			V _{CC} = 6.0 V		23	
		T _C = -55°C, +125°C C _L = 50 pF See figure 5	V _{CC} = 2.0 V	10, 11	198	
			V _{CC} = 4.5 V		40	
			V _{CC} = 6.0 V		34	
Propagation delay time, LOAD to Qn <u>3/</u>	t _{PHL2} , t _{PLH2}	T _C = +25°C C _L = 50 pF See figure 5	V _{CC} = 2.0 V	9	264	ns
			V _{CC} = 4.5 V		53	
			V _{CC} = 6.0 V		45	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.						
Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, <u>LOAD</u> to Qn 3/	t _{PHL2} , t _{PLH2}	T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		396	ns
					79	
					67	
Propagation delay time, Dn to Qn 3/	t _{PHL3} , t _{PLH3}	T _C = +25°C C _L = 50 pF See figure 5	9		240	ns
					48	
					41	
		T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		360	
					72	
					61	
Propagation delay time, CLK to Qn 3/	t _{PHL4} , t _{PLH4}	T _C = +25°C C _L = 50 pF See figure 5	9		215	ns
					43	
					37	
		T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		325	
					65	
					55	
See footnotes at end of table.						
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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, CLK to RC 3/	t _{PHL5} , t _{PLH5}	T _C = +25°C C _L = 50 pF See figure 5	9		125	ns
					25	
					21	
		T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		190	
					38	
					32	
Propagation delay time, Down/Up to RC 3/	t _{PHL6} , t _{PLH6}	T _C = +25°C C _L = 50 pF See figure 5	9		228	ns
					46	
					38	
		T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		342	
					68	
					59	
Propagation delay time, CLK to MAX/MIN 3/	t _{PHL7} , t _{PLH7}	T _C = +25°C C _L = 50 pF See figure 5	9		255	ns
					51	
					43	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, CLK to MAX/MIN 3/	t _{PHL7} , t _{PLH7}	T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		385	ns
					77	
					65	
Propagation delay time, Down/Up to MAX/MIN 3/	t _{PHL8} , t _{PLH8}	T _C = +25°C C _L = 50 pF See figure 5	9		190	ns
					38	
					32	
		T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		285	
					57	
					48	
Output transition time, Qn, MAX/MIN, RC 3/ 4/	t _{THL1} , t _{TLH1}	T _C = +25°C C _L = 50 pF See figure 5	9		75	ns
					15	
					13	

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Output transition time, Qn, MAX/MIN, RC 3/ 4/	t _{THL} , t _{TLH}	T _C = -55°C, +125°C C _L = 50 pF See figure 5	10, 11		110	ns
					22	
					19	
Maximum input capacitance	C _{IN}	See 4.3.1c, V _{CC} = GND	4		10	pF

1/ For a power supply of 5.0 V ±10%, the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V). The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 80 pF, determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

2/ V_{IH} and V_{IL} tests are not required if applied as forcing functions for the V_{OH} and V_{OL} tests.

3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified limit in table I.

4/ Transition times (t_{THL}, t_{TLH}), if not tested, shall be guaranteed to the specified limits in table I.

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Device type	01	
Case outlines	E	2
Terminal number	Terminal symbol	
1	DB	NC
2	QB	DB
3	QA	QB
4	ENABLE	QA
5	DOWN/UP	ENABLE
6	QC	NC
7	QD	DOWN/UP
8	GND	QC
9	DD	QD
10	DC	GND
11	LOAD	NC
12	MAX/MIN	DD
13	RC	DC
14	CLK	LOAD
15	DA	MAX/MIN
16	VCC	NC
17	---	RC
18	---	CLK
19	---	DA
20	---	VCC

NC = No connect

FIGURE 1. Terminal connections.

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Mode select table

LOAD	ENABLE	DOWN/ UP	CLK	FUNCTION
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Load
H	H	X	X	No change

RC truth table

Inputs			Output
ENABLE	MAX/MIN	CK	RC
L	H	L	L
L	L	L	H
L	H	H	H
L	L	H	H
H	L	H	H
H	L	L	H

H = High level

L = Low level

X = Irrelevant

 = Transition from low to high

Asynchronous inputs Low input to load sets QA = A,

QB = B, QC = C, QD = D

FIGURE 2. Truth tables.

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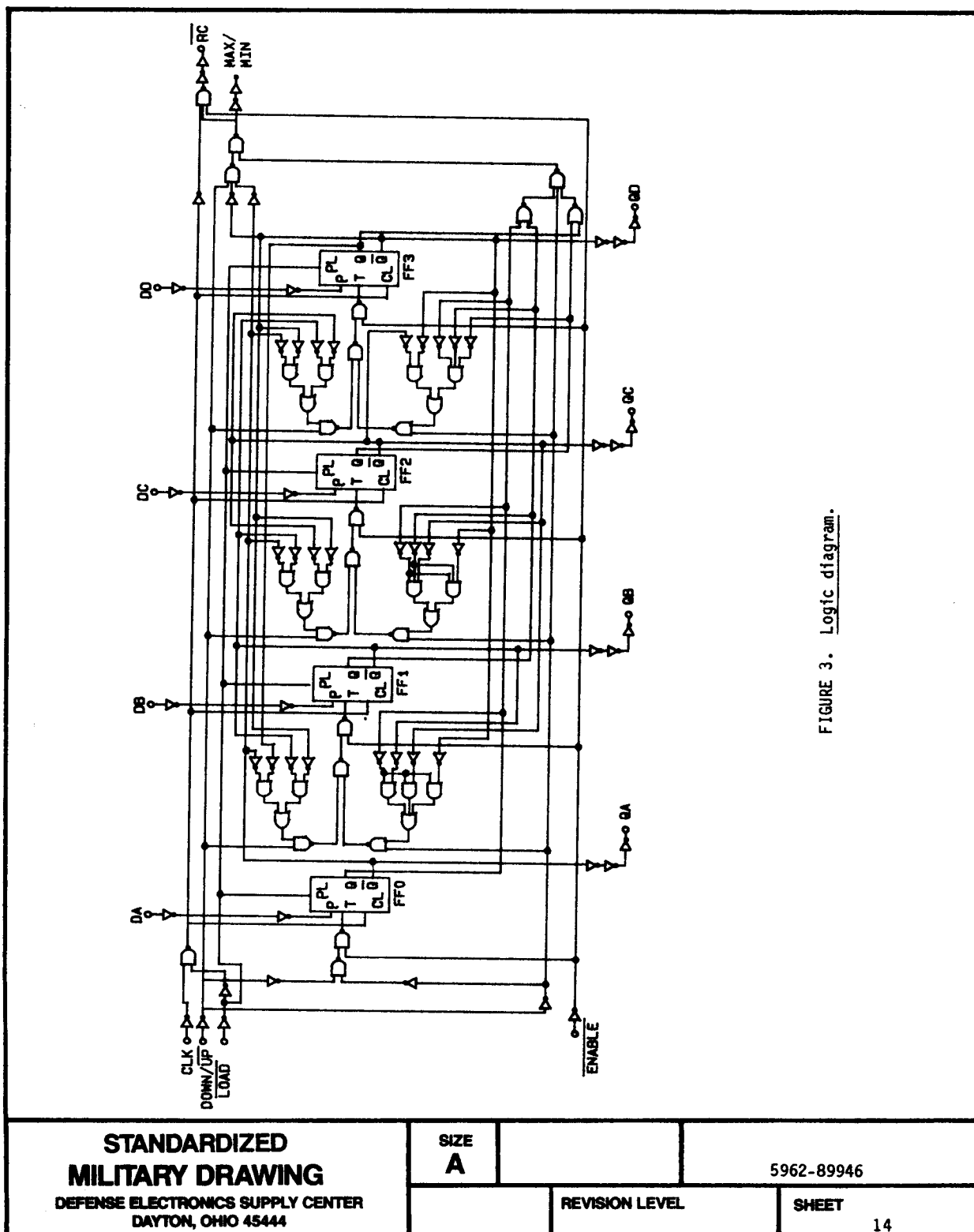
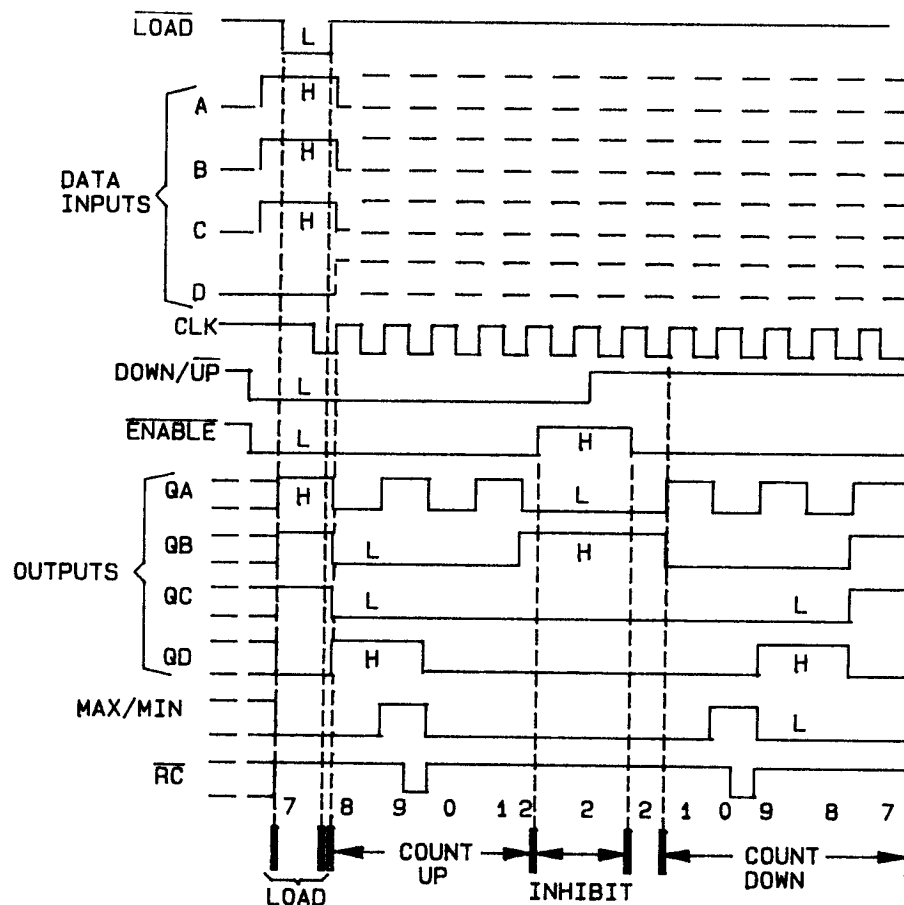


FIGURE 3. Logic diagram.

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Sequence:

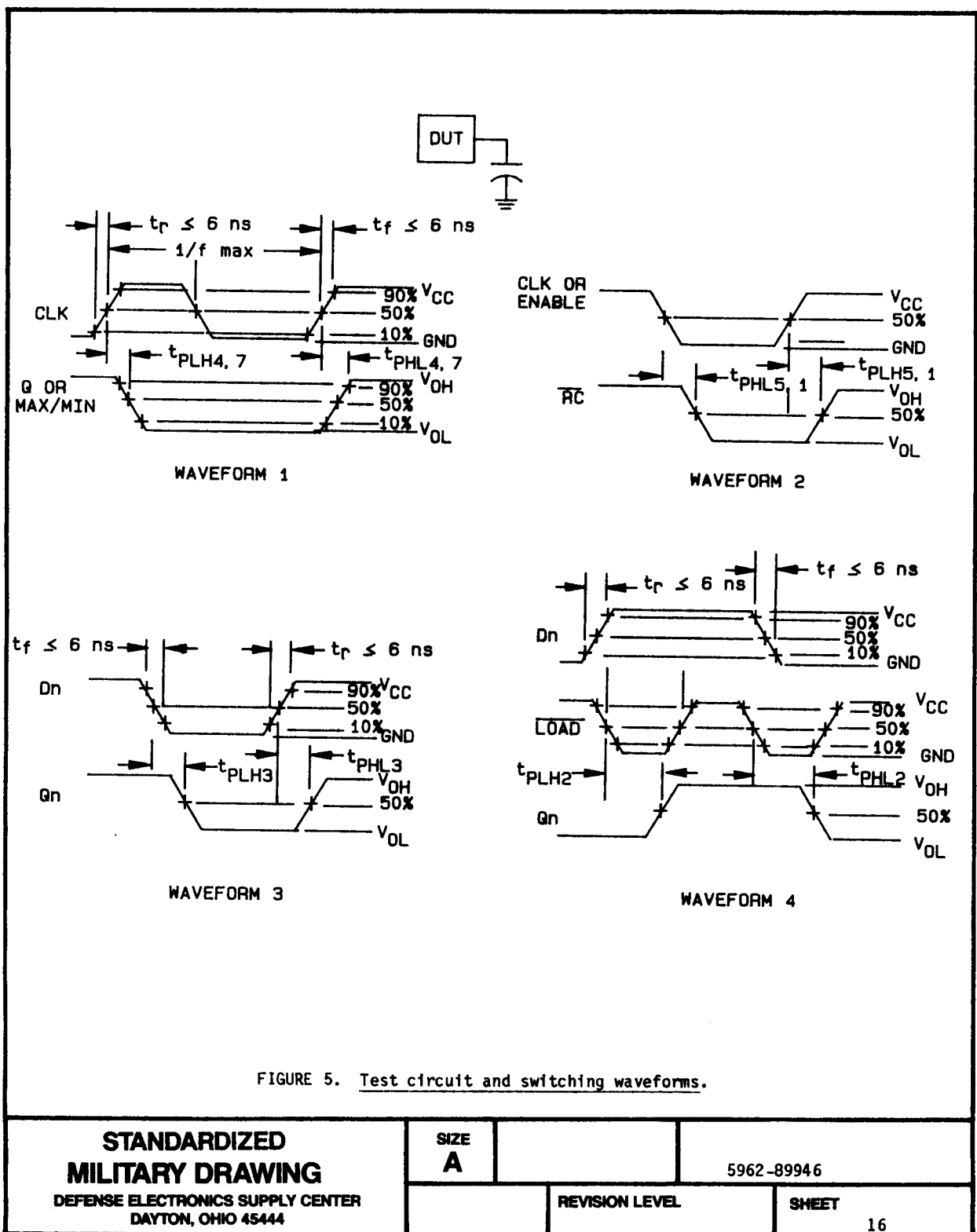
- (1) Load (preset) to BCD seven
- (2) Count up to eight, nine, zero, one, and two
- (3) Inhibit
- (4) Count down to one, zero, nine, eight, and seven

FIGURE 4. Counting sequence diagram.

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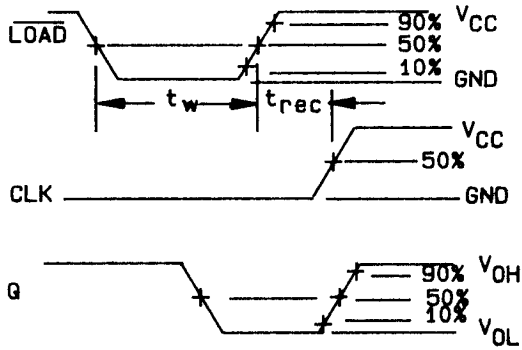
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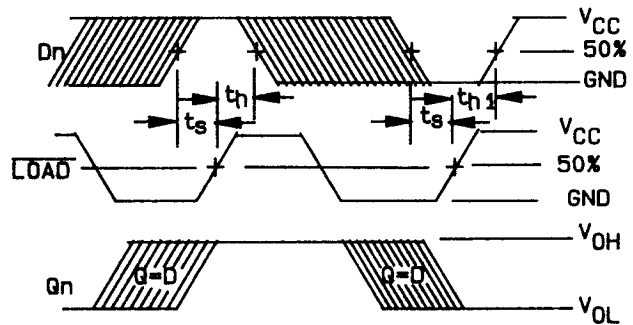


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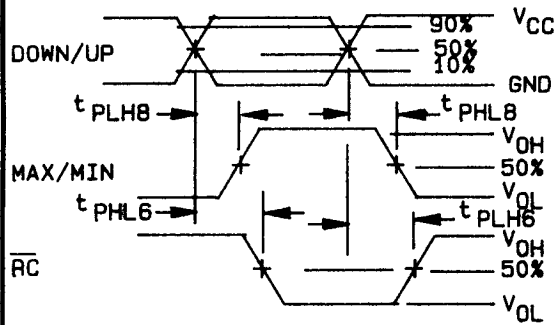
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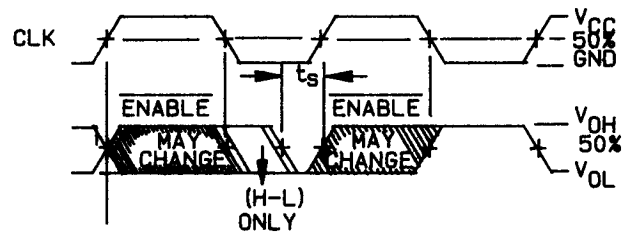
WAVEFORM 5



WAVEFORM 6



WAVEFORM 7



WAVEFORM 8

The shaded area indicate when the input is permitted to change for predictable output performance.

FIGURE 5. Test circuit and switching waveforms - Continued.

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3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{in} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

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6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number ^{1/}
5962-8994601EX	01295 34371	SNJ54HC190J CD54HC190F/3A
5962-89946012X	01295	SNJ54HC190FK

^{1/} Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

01295

34371

Vendor name
and address

Texas Instruments Incorporated
13500 N. Central Expressway
PO Box 655303
Dallas, TX 75265
Point of contact: I-20 at FM 1788
Midland, TX 79711-0448

Harris Semiconductor
2401 Palm Bay Road
PO Box 883
Melbourne, FL 32901

**STANDARDIZED
MILITARY DRAWING**

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
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