



M40Z111 M40Z111W

5V OR 3V NVRAM SUPERVISOR FOR UP TO TWO LPSRAMs

FEATURES SUMMARY

- CONVERT LOW POWER SRAMs INTO NVRAMs
- PRECISION POWER MONITORING and POWER SWITCHING CIRCUITRY
- AUTOMATIC WRITE-PROTECTION WHEN V_{CC} IS OUT-OF-TOLERANCE
- CHOICE OF SUPPLY VOLTAGES and POWER-FAIL DESELECT VOLTAGES:
 - M40Z111: $V_{CC} = 4.5$ to $5.5V$
THS = V_{SS} ; $4.5 \leq V_{PFD} \leq 4.75V$
THS = V_{OUT} ; $4.2 \leq V_{PFD} \leq 4.5V$
 - M40Z111W: $V_{CC} = 3.0$ to $3.6V$
THS = V_{SS} ; $2.8 \leq V_{PFD} \leq 3.0V$
 $V_{CC} = 2.7$ to $3.3V$
THS = V_{OUT} ; $2.5 \leq V_{PFD} \leq 2.7V$
- LESS THAN 15ns CHIP ENABLE ACCESS PROPAGATION DELAY (for 5.0V device)
- PACKAGING INCLUDES A 28-LEAD SOIC and SNAPHAT® TOP (to be ordered separately)
- SOIC PACKAGE PROVIDES DIRECT CONNECTION FOR A SNAPHAT TOP WHICH CONTAINS THE BATTERY

Figure 1. 28-pin SOIC Package

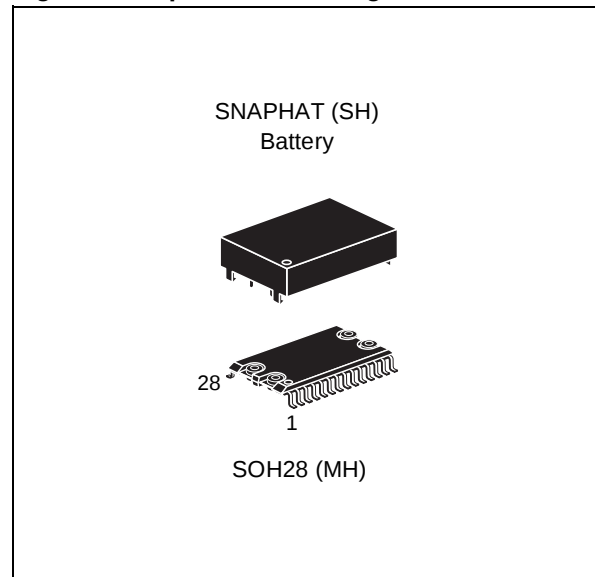


TABLE OF CONTENTS

SUMMARY DESCRIPTION	3
Logic Diagram (Figure 2.)	3
Signal Names (Table 1.)	3
SOIC28 Connections (Figure 3.)	3
Hardware Hookup (Figure 4.)	4
MAXIMUM RATING	4
Absolute Maximum Ratings (Table 2.)	4
DC AND AC PARAMETERS	5
DC and AC Measurement Conditions (Table 3.)	5
AC Testing Load Circuit (Figure 5.)	5
Capacitance (Table 4.)	5
DC Characteristics (Table 5.)	6
OPERATION	7
Data Retention Lifetime Calculation	7
Power Down Timing (Figure 6.)	8
Power Up Timing (Figure 7.)	8
Power Down/Up AC Characteristics (Table 6.)	9
V _{CC} Noise And Negative Going Transients	9
Supply Voltage Protection (Figure 8.)	9
PART NUMBERING	10
Battery Table (Table 8.)	10
PACKAGE MECHANICAL INFORMATION	11
REVISION HISTORY	14

SUMMARY DESCRIPTION

The M40Z111/W NVRAM SUPERVISOR is a self-contained device which converts a standard low-power SRAM into a non-volatile memory. A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition. When an invalid V_{CC} condition occurs, the conditioned chip enable ($\overline{E}_{CON}$) output is forced inactive to write-protect the stored data in the SRAM. During a power failure, the SRAM is switched from the V_{CC} pin to the lithium cell within the SNAPHAT[®] to provide the energy required for data retention. On a subsequent power-up, the SRAM remains write protected until a valid power condition returns. The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct con-

nection to a separate SNAPHAT housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion. The SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28-lead SOIC, the battery package (e.g., SNAPHAT) part number is "M4Z28-BR00SH" or "M4Z32-BR00SH" (See Table 8, page 10).

Figure 2. Logic Diagram

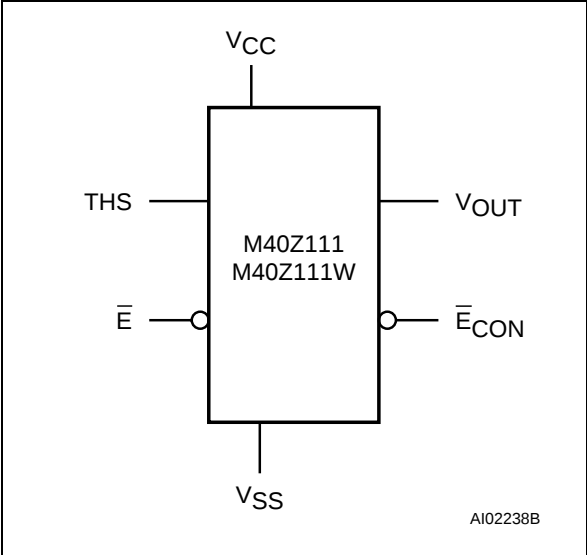


Table 1. Signal Names

THS	Threshold Select Input
$\overline{E}$	Chip Enable Input
$\overline{E}_{CON}$	Conditioned Chip Enable Output
V_{OUT}	Supply Voltage Output
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. SOIC28 Connections

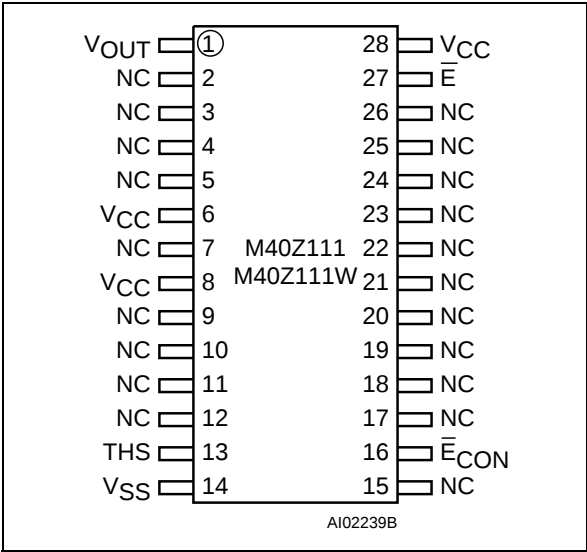
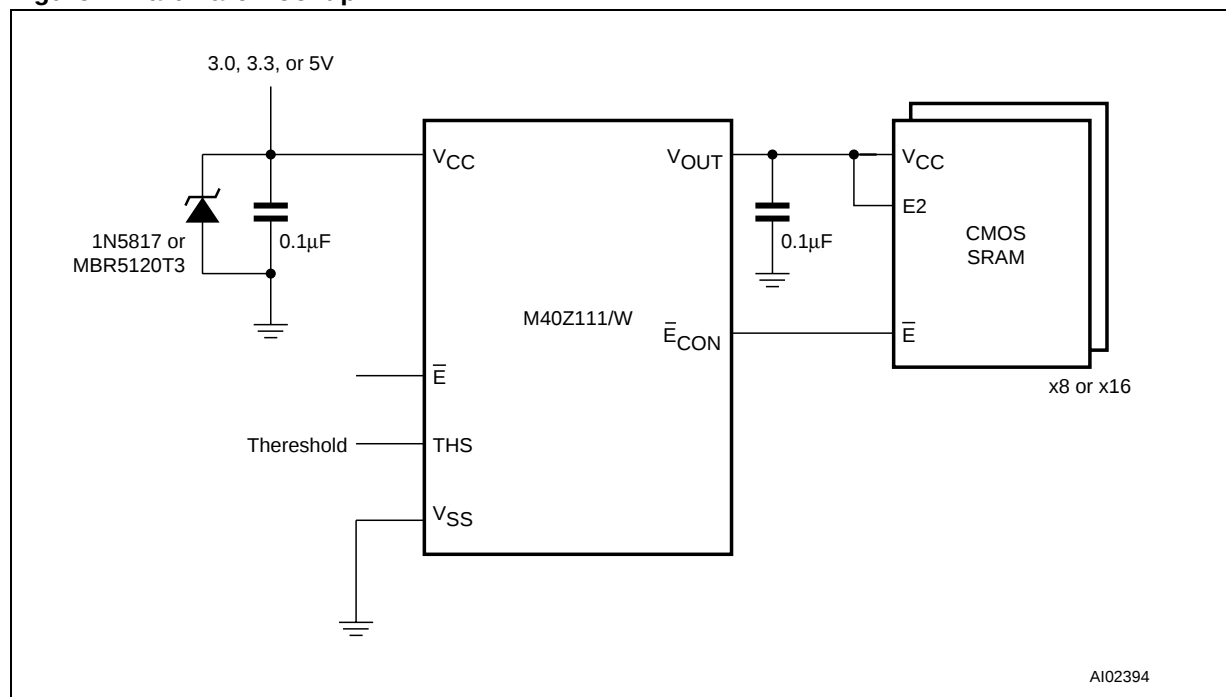


Figure 4. Hardware Hookup



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T _A	Ambient Operating Temperature	Grade 6	−40 to 85	°C
T _{STG}	Storage Temperature (V _{CC} Off)	SNAPHAT®	−40 to 85	°C
		SOIC	−55 to 125	°C
T _{SLD} ⁽¹⁾	Lead Solder Temperature for 10 seconds		260	°C
V _{IO}	Input or Output Voltages		−0.3 to V _{CC} +0.3	V
V _{CC}	Supply Voltage	M40Z111	−0.3 to 7.0	V
		M40Z111W	−0.3 to 4.6	V
I _O	Output Current		20	mA
P _D	Power Dissipation		1	W

Note: 1. Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).

CAUTION: Negative undershoots below −0.3V are not allowed on any pin while in the Battery Back-up mode.

CAUTION: Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

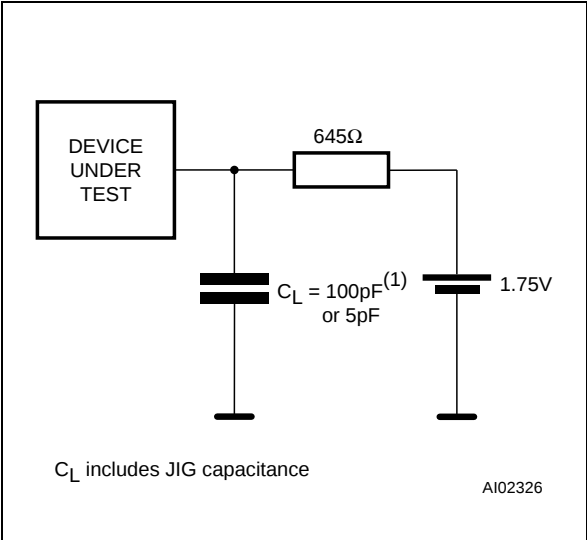
ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. DC and AC Measurement Conditions

Parameter	M40Z111	M40Z111W
V _{CC} Supply Voltage	4.5 to 5.5V	2.7 to 3.6V
Ambient Operating Temperature	–40 to 85°C	–40 to 85°C
Load Capacitance (C _L)	100pF	50pF
Input Rise and Fall Times	≤ 5ns	≤ 5ns
Input Pulse Voltages	0 to 3V	0 to 3V
Input and Output Timing Ref. Voltages	1.5V	1.5V

Note: Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Load Circuit



Note: 1. 50pF for M40Z111W.

Table 4. Capacitance

Symbol	Parameter ^(1,2)	Min	Max	Unit
C _{IN}	Input Capacitance		8	pF
C _{OUT} ⁽³⁾	Output Capacitance		10	pF

Note: 1. Effective capacitance measured with power supply at 5V (M40Z111) or 3.3V (M40Z111W); sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected

Table 5. DC Characteristics

Sym	Parameter	Test Condition ⁽¹⁾	M40Z111			M40Z111W			Unit
			Min	Typ	Max	Min	Typ	Max	
I _{CC}	Supply Current	Outputs open		3	6		2	4	mA
I _{CCDR}	Data Retention Mode Current				150			150	nA
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}			±1			±1	μA
I _{LO} ⁽²⁾	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC}			±1			±1	μA
I _{OUT1}	V _{OUT} Current (Active)	V _{OUT} > V _{CC} - 0.3			160			100	mA
		V _{OUT} > V _{CC} - 0.2			100			65	mA
I _{OUT2}	V _{OUT} Current (Battery Back-up)	V _{OUT} > V _{BAT} - 0.3		100			100		μA
V _{BAT}	Battery Voltage		2.0	3.0	3.5	2.0	3.0	3.5	V
V _{IH}	Input High Voltage		2.2		V _{CC} + 0.3	2.0		V _{CC} + 0.3	V
V _{IL}	Input Low Voltage		-0.3		0.8	-0.3		0.8	V
V _{OH}	Output High Voltage	I _{OH} = -2.0mA	2.4			2.4			V
V _{OHB}	V _{OH} Battery Back-up	I _{OUT2} = -1.0μA	2.0	2.9	3.6	2.0	2.9	3.6	V
V _{OL}	Output Low Voltage	I _{OL} = 4.0mA			0.4			0.4	V
THS	Threshold Select Voltage		V _{SS}		V _{OUT}	V _{SS}		V _{OUT}	V
V _{PF}	Power-fail Deselect Voltage (THS = V _{SS})		4.50	4.60	4.75	2.80	2.90	3.00	V
	Power-fail Deselect Voltage (THS = V _{OUT})		4.20	4.35	4.50	2.50	2.60	2.70	V
V _{SO}	Battery Back-up Switchover Voltage			3.0			V _{PF} - 100mV		V

Note: 1. Valid for Ambient Operating Temperature: T_A = -40 to 85°C; V_{CC} = 4.5 to 5.5V or 2.7 to 3.6V (except where noted).
2. Outputs deselected.

OPERATION

The M40Z111/W, as shown in Figure 4, page 4, can control up to two standard low-power SRAMs. These SRAMs must be configured to have the chip enable input disable all other input signals. Most slow, low-power SRAMs are configured like this, however many fast SRAMs are not. During normal operating conditions, the conditioned chip enable ($\overline{E_{CON}}$) output pin follows the chip enable ($\overline{E}$) input pin with timing shown in Table 6, page 9. An internal switch connects V_{CC} to V_{OUT} . This switch has a voltage drop of less than 0.3V (I_{OUT1}).

When V_{CC} degrades during a power failure, $\overline{E_{CON}}$ is forced inactive independent of $\overline{E}$. In this situation, the SRAM is unconditionally write protected as V_{CC} falls below an out-of-tolerance threshold (V_{PFD}). The power fail detection value associated with V_{PFD} is selected by the THS pin and is shown in Table 5, page 6.

Note: The THS pin must be connected to either V_{SS} or V_{OUT} .

If chip enable access is in progress during a power fail detection, that memory cycle continues to completion before the memory is write protected. If the memory cycle is not terminated within time t_{WP} , $\overline{E_{CON}}$ is unconditionally driven high, write protecting the SRAM.

A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the SRAM's contents. At voltages below V_{PFD} (min), the user can be assured the memory will be write protected provided the V_{CC} fall time exceeds t_F .

As V_{CC} continues to degrade, the internal switch disconnects V_{CC} and connects the internal battery to V_{OUT} . This occurs at the switchover voltage (V_{SO}). Below the V_{SO} , the battery provides a voltage V_{OHB} to the SRAM and can supply current I_{OUT2} (see Table 5, page 6). When V_{CC} rises

above V_{SO} , V_{OUT} is switched back to the supply voltage. Output $\overline{E_{CON}}$ is held inactive for t_{ER} (200ms maximum) after the power supply has reached V_{PFD} , independent of the $\overline{E}$ input, to allow for processor stabilization (see Figure 7, page 8).

Data Retention Lifetime Calculation

Most low power SRAMs on the market today can be used with the M40Z111/W NVRAM SUPERVISOR. There are, however some criteria which should be used in making the final choice of which SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M40Z111/W and SRAMs to be "Don't Care" once V_{CC} falls below V_{PFD} (min). The SRAM should also guarantee data retention down to $V_{CC} = 2.0V$. The chip enable access time must be sufficient to meet the system needs with the chip enable propagation delays included. If the SRAM includes a second chip enable pin ($\overline{E2}$), this pin should be tied to V_{OUT} . If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0V.

Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{CCDR} value of the M40Z111/W to determine the total current requirements for data retention.

The available battery capacity for the SNAPHAT® of your choice can then be divided by this current to determine the amount of data retention available (see Table 8, page 10). For more information on Battery Storage Life refer to the Application Note AN1012.

Figure 6. Power Down Timing

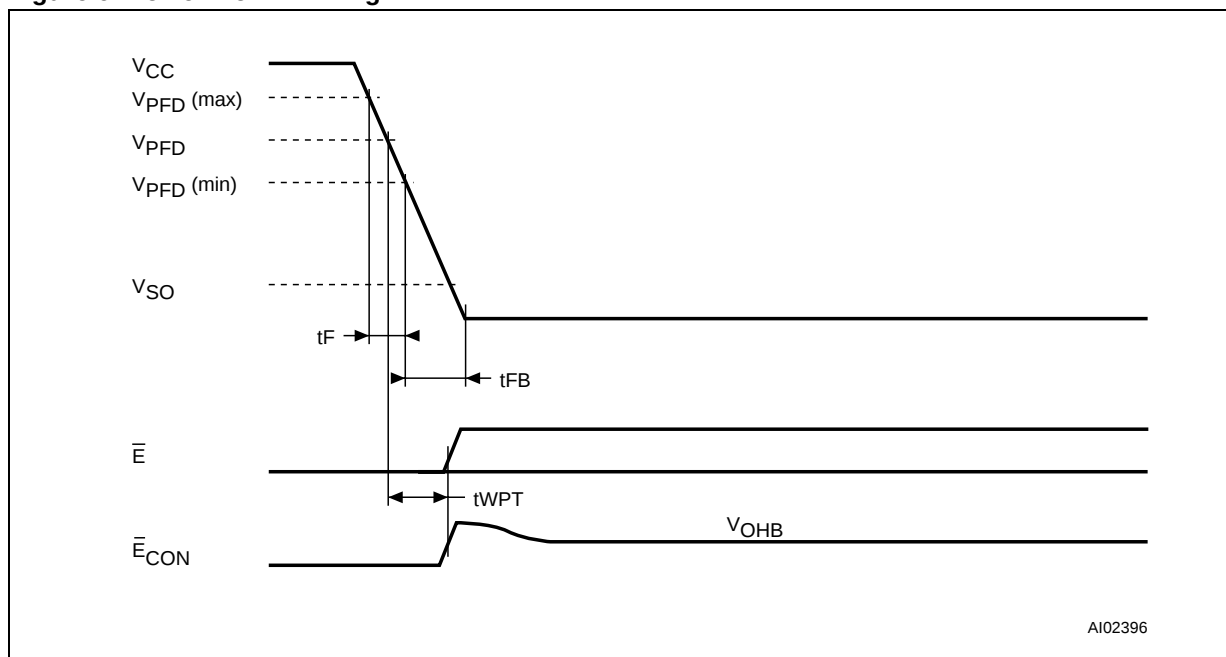


Figure 7. Power Up Timing

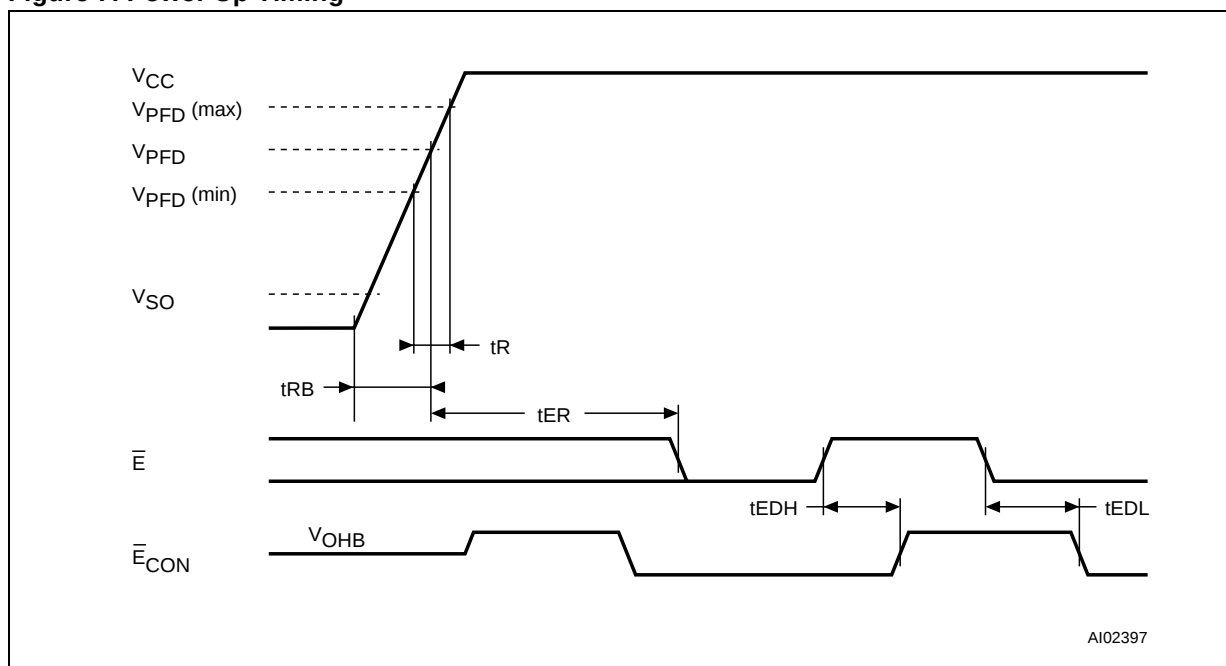


Table 6. Power Down/Up AC Characteristics

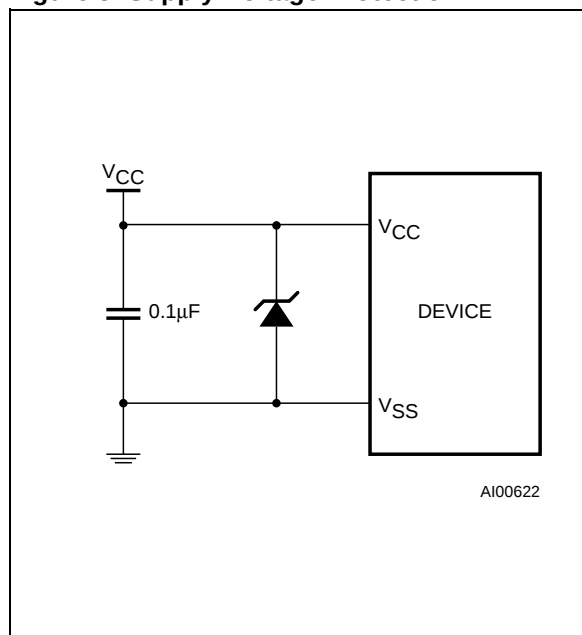
Symbol	Parameter ⁽¹⁾		Min	Max	Unit
$t_F^{(2)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ V_{CC} Fall Time		300		μs
$t_{FB}^{(3)}$	$V_{PFD}(\text{min})$ to V_{SS} V_{CC} Fall Time		10		μs
t_R	$V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ V_{CC} Rise Time		10		μs
t_{RB}	V_{SS} to $V_{PFD}(\text{min})$ V_{CC} Rise Time		1		μs
t_{EDL}	Chip Enable Propagation Delay	M40Z111		15	ns
		M40Z111W		20	ns
t_{EDH}	Chip Enable Propagation Delay	M40Z111		10	ns
		M40Z111W		20	ns
$t_{ER}^{(4)}$	Chip Enable Recovery		40	200	ms
t_{WPT}	Write Protect Time	M40Z111	40	150	μs
		M40Z111W	40	250	μs

Note: 1. Valid for Ambient Operating Temperature: $T_A = -40$ to 85°C ; $V_{CC} = 4.5$ to 5.5V or 2.7 to 3.6V (except where noted).
2. $V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ fall time of less than t_F may result in deselection/write protection not occurring until $200\text{ }\mu\text{s}$ after V_{CC} passes $V_{PFD}(\text{min})$.
3. $V_{PFD}(\text{min})$ to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.
4. $t_{ER}(\text{min}) = 20\text{ms}$ for Industrial Temperature Range - Grade 6 device.

V_{CC} Noise And Negative Going Transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of $0.1\mu\text{F}$ (as shown in Figure 8) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC} , anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBR120T3 is recommended for surface mount.

Figure 8. Supply Voltage Protection


PART NUMBERING

Table 7. Ordering Information Scheme

Example:	M40Z	111W	MH	6	TR
Device Type					
M40Z					
Supply Voltage and Write Protect Voltage					
111 = $V_{CC} = 4.5$ to $5.5V$; $V_{PFD} = 4.3$ to $4.5V$					
THS = $V_{SS} = 4.5 \leq V_{PFD} \leq 4.75V$					
THS = $V_{OUT} = 4.2 \leq V_{PFD} \leq 4.5V$					
111W = $V_{CC} = 2.7$ to $3.6V$; $V_{PFD} = 2.6$ to $2.7V$					
THS = $V_{SS} = 2.8 \leq V_{PFD} \leq 3.0V$					
$V_{CC} = 2.7$ to $3.3V$					
THS = $V_{OUT} = 2.5 \leq V_{PFD} \leq 2.7V$					
Package					
MH ⁽¹⁾ = SOH28					
Temperature Range					
6 = -40 to $85^{\circ}C$					
Shipping Method for SOIC					
blank = Tubes					
TR = Tape & Reel					

Note: 1. The SOIC package (SOH28) requires the battery package (SNAPHAT[®]) which is ordered separately under the part number "M4ZXX-BR00SHX" in plastic tube or "M4ZXX-BR00SHXTR" in Tape & Reel form.

Caution: Do not place the SNAPHAT battery package "M4ZXX-BR00SH" in conductive foam as this will drain the lithium button-cell battery.

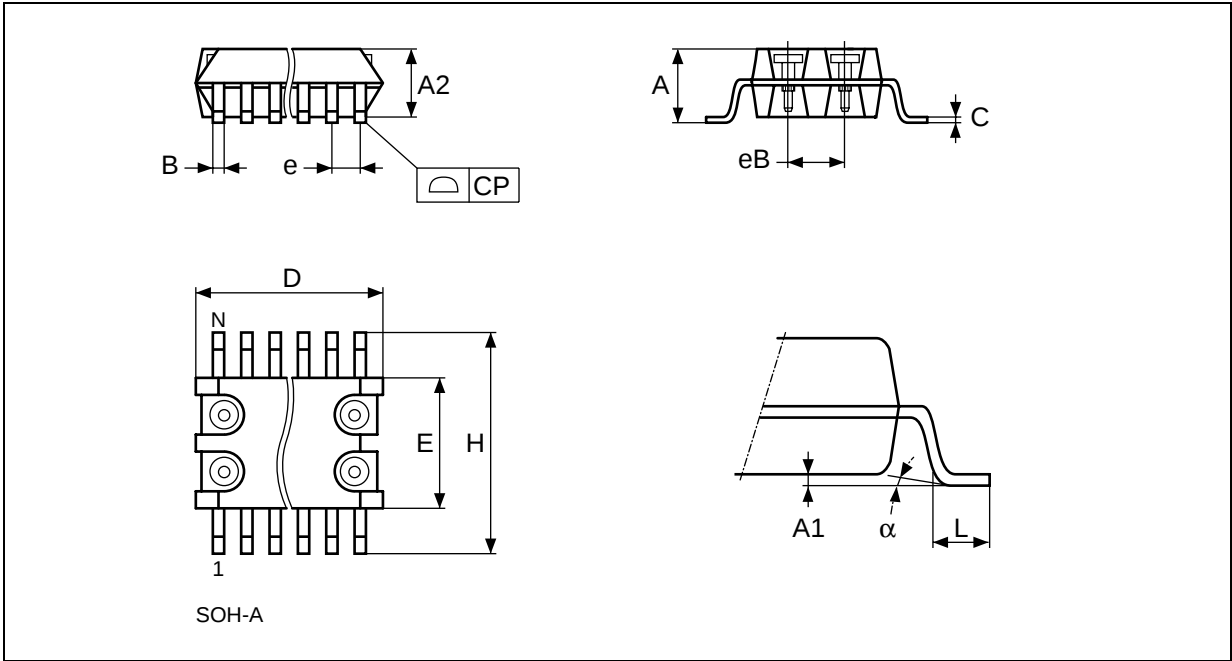
For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 8. Battery Table

Part Number	Description	Package
M4Z28-BR00SH	SNAPHAT Housing for 48mAh Battery	SH
M4Z32-BR00SH	SNAPHAT Housing for 120mAh Battery	SH

PACKAGE MECHANICAL INFORMATION

Figure 9. SOH28 – 28-lead Plastic Small Outline, 4-socket battery SNAPHAT, Package Outline

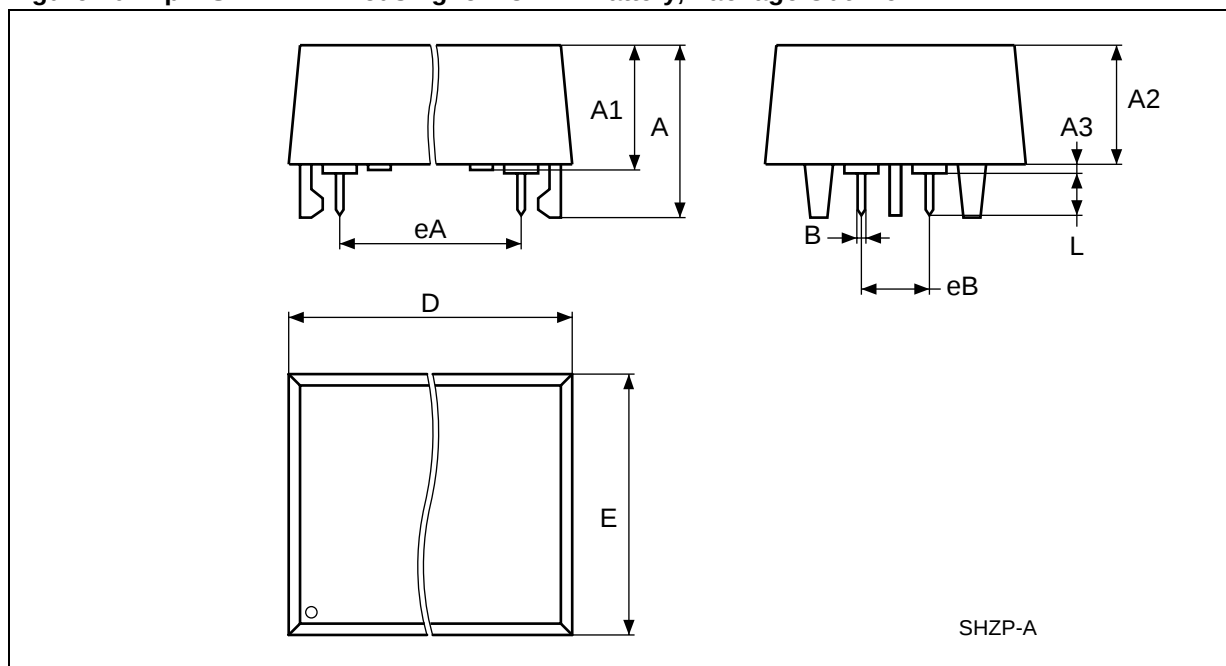


Note: Drawing is not to scale.

Table 9. SOH28 – 28-lead Plastic Small Outline, battery SNAPHAT, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 10. 4-pin SNAPHAT Housing for 48mAh Battery, Package Outline

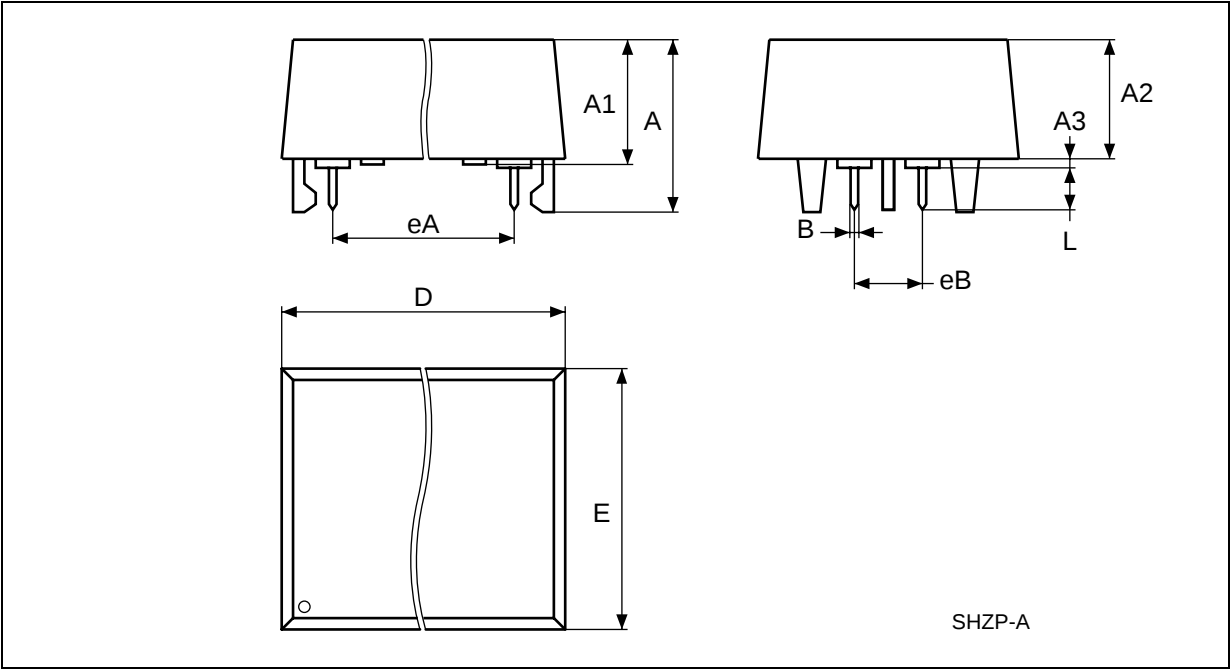


Note: Drawing is not to scale.

Table 10. 4-pin SNAPHAT Housing for 48mAh Battery, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 11. 4-pin SNAPHAT Housing for 120mAh Battery, Package Outline



Note: Drawing is not to scale.

Table 11. 4-pin SNAPHAT Housing for 120mAh Battery, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

REVISION HISTORY

Table 12. Document Revision History

Date	Revision Details
September 2000	First Draft Issue
09/14/01	Reformatted, TOC added, changed DC Characteristics (Table 5); changed battery, ind. temperature information (Tables 2, 6, 7, 8, Figures 10, 11); Corrected SOIC label (Figure 3); added E2 to Hookup (Figure 4)
05/13/02	Modify reflow time and temperature footnote (Table 2)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
All other names are the property of their respective owners.

© 2002 STMicroelectronics - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia -
Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

www.st.com