REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to table I. Editorial changes throughout.	89-10-16	M.A. Frye
B	Add device types 05 and 06. Add case outline "U" to drawing. Removed vendor CAGE 61772 as source of supply for case outline Y. Changes to table I. Editorial changes throughout.	92-05-14	M.A. Frye
C	Add device types 07 through 12. Remove vendor CAGE 61772 as source of supply for device types 01 through 06 and add vendor CAGE 61772 as source of supply for device types 07 through 12. Add notes 6/ and 7/ to table I. Add notes to BUSY cycle waveforms. Editorial changes throughout.	93-09-16	M.A. Frye
D	Changes in accordance with NOR 5962-R132-94.	94-03-30	M. A. Frye
E	Changes to table I a.c. parameters based on updated die. Updated boilerplate. - glg	99-12-01	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

SHEET																				
REV	E	E	E	E	E	E	E	E												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
James E. Jamison

CHECKED BY
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APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-12-12

REVISION LEVEL
E

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 2K X 16 DUAL PORT SRAM, MONOLITHIC SILICON

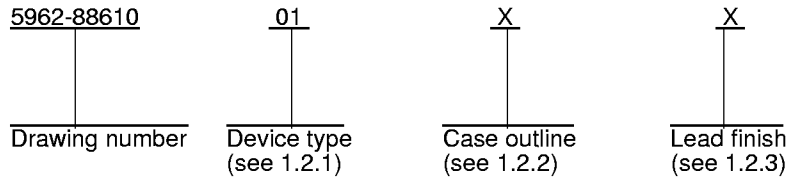
SIZE	CAGE CODE	
A	**67268**	**5962-88610**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(see 6.6)	2K x 16 dual port CMOS SRAM (master)	90 ns
02	(see 6.6)	2K x 16 dual port CMOS SRAM (slave)	90 ns
03	(see 6.6)	2K x 16 dual port CMOS SRAM (master)	70 ns
04	(see 6.6)	2K x 16 dual port CMOS SRAM (slave)	70 ns
05	(see 6.6)	2K x 16 dual port CMOS SRAM (master)	55 ns
06	(see 6.6)	2K x 16 dual port CMOS SRAM (slave)	55 ns
07	(see 6.6)	2K x 16 dual port CMOS SRAM (master)	90 ns
08	(see 6.6)	2K x 16 dual port CMOS SRAM (slave)	90 ns
09	(see 6.6)	2K x 16 dual port CMOS SRAM (master)	70 ns
10	(see 6.6)	2K x 16 dual port CMOS SRAM (slave)	70 ns
11	(see 6.6)	2K x 16 dual port CMOS SRAM (master)	55 ns
12	(see 6.6)	2K x 16 dual port CMOS SRAM (slave)	55 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	68	flat pack
X	See figure 1	68	dual-in-line package
Y	CQCC1-N68	68	square leadless chip carrier
Z	CMGA3-68	68	pin grid array

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +6.0 V dc
DC output current	50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	2.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases U and X	37°C/W
Cases Y and Z	See MIL-STD-1835
Junction temperature (T_J)	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.2 V dc to 6.0 V dc
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 2/
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.
2/ V_{IL}(min) = -3.0 V dc for pulse width less than 20 ns.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V		1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V	I/O_0 - I/O_{15} I_{OL} = 4.0 mA	1, 2, 3	All		0.4	V
			$\overline{BUSY}$ I_{OL} = 16 mA	1, 2, 3	All		0.5	V
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5 V, GND $\le V_{IN} \le V_{CC}$		1, 2, 3	All		10	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}, GND $\le V_{OUT} \le V_{CC}$		1, 2, 3	All		10	µA
Dynamic operating current (both ports active)	I_{CC}	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IL}, f = f_{MAX} 1/, outputs open		1, 2, 3	01-04		260	mA
					05,06		280	
					07-10		310	
					11-12		315	
Standby power supply current (both ports-TTL input levels)	I_{SB1}	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, V_{CC} = 5.5 V, f = f_{MAX} 1/,		1, 2, 3	01-04		75	mA
					05,06		80	
Standby power supply current (one port-TTL input levels)	I_{SB2}	V_{CC} = 5.5 V, $\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, f = f_{MAX} 1/, active port outputs open		1, 2, 3	01-04		170	mA
					05,06		180	
					07-10		200	
					11,12		210	
Full standby power supply current (both ports-CMOS input levels)	I_{SB3}	V_{CC} = 5.5 V, f = 0 1/, $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ -0.2 V, $V_{IN} \ge V_{CC}$ -0.2 V or $\le$ 0.2 V		1, 2, 3	All		30	mA
Full standby power supply current (one port-CMOS input levels)	I_{SB4}	V_{CC} = 5.5 V, f_{MAX} 1/ $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ -0.2 V, $V_{IN} \ge V_{CC}$, -0.2 V or $\le$ 0.2 V, active port outputs open		1, 2, 3	01,02		155	mA
					03,04		160	
					05,06		170	
					07-10		190	
					11,12		200	
Input capacitance	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, see 4.3.1c		4	All		11	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, $V_{I/O}$ = 0 V, f = 1.0 MHz, T_A = +25°C, See 4.3.1c	4	All		11	pF
Functional tests		See 4.3.1d	7, 8A, 8B	All			
Read cycle time	t_{RC}	See figures 5 and 6. 2/	9, 10, 11	01,02,07,08	90		ns
				03,04,09,10	70		
				05,06,11,12	55		
Address access time	t_{AA}	See figures 5 and 6. 2/	9, 10, 11	01,02,07,08		90	ns
				03,04,09,10		70	
				05,06,11,12		55	
Output hold from address change	t_{OH}	See figures 5 and 6. 2/	9, 10, 11	All	0		ns
Chip enable access time	t_{ACE}	See figures 5 and 6. 2/	9, 10, 11	01,02,07,08		90	ns
				03,04,09,10		70	
				05,06 11,12		55	
Output enable access time	t_{AOE}	See figures 5 and 6. 2/	9, 10, 11	01-04,07-10		40	ns
				05,06,11,12		35	
Output low Z time	t_{LZ}	See figures 5 and 6. 3/ 4/	9, 10, 11	All	5.0		ns
Output high Z time	t_{HZ}	See figures 5 and 6. 3/ 4/	9, 10, 11	01-04,07-10		25	ns
				05,06,11,12		20	
Chip enable to power-up time	t_{PU}	See figures 5 and 6. 2/ 3/	9, 10, 11	All	0		ns
Chip disable to power-down time	t_{PD}	See figures 5 and 6. 2/ 3/	9, 10, 11	All		50	ns
Write cycle time 5/	t_{WC}	See figures 5 and 7. 2/	9, 10, 11	01,02,07,08	90		ns
				03,04,09,10	70		
				05,06,11,12	55		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable to end of write	t_{EW}	See figures 5 and 7. 2/	9, 10, 11	01-04, 07-10	50		ns
				05,06, 11,12	40		
Address valid to end of write	t_{AW}	See figures 5 and 7. 2/	9, 10, 11	01-04, 07-10	50		ns
				05,06, 11,12	40		
Address setup time	t_{AS}	See figures 5 and 7. 2/	9, 10, 11	All	0		ns
Write pulse width 6/	t_{WP}	See figures 5 and 7. 2/	9, 10, 11	01-02, 07-10	50		ns
				05,06 11,12	40		
Write recovery time	t_{WR}	See figures 5 and 7. 2/	9, 10, 11	All	0		ns
Data valid to end of write	t_{DW}	See figures 5 and 7. 2/	9, 10, 11	01,02, 07,08	30		ns
				03,04, 09-12	25		
				05,06	20		
Output high Z time	t_{HZ}	See figures 5 and 7. 3/ 4/	9, 10, 11	01-04, 07-10		25	ns
				05,06, 11,12		20	
Data hold time 7/	t_{DH}	See figures 5 and 7. 2/	9, 10, 11	All	5.0		ns
Write enable to output in high Z	t_{WZ}	See figures 5 and 7. 3/ 4/	9, 10, 11	01-04, 07-10		25	ns
				05,06, 11,12		20	
Output active from end of write 7/	t_{OW}	See figures 5 and 7. 3/ 4/	9, 10, 11	01-04	0		ns
				05-12	5		
Write to $\overline{\text{BUSY}}$ 8/	t_{WB}	See figures 5 and 8. 2/	9, 10, 11	02,04, 06,08, 10,12	0		ns
Write hold after $\overline{\text{BUSY}}$ 9/	t_{WH}	See figures 5 and 8. 2/	9, 10, 11	02,04, 06,08, 10,12	30		ns
$\overline{\text{BUSY}}$ access time to address	t_{BAA}	See figures 5 and 8. 2/	9, 10, 11	01,03, 07,09		45	ns
				05,11		40	

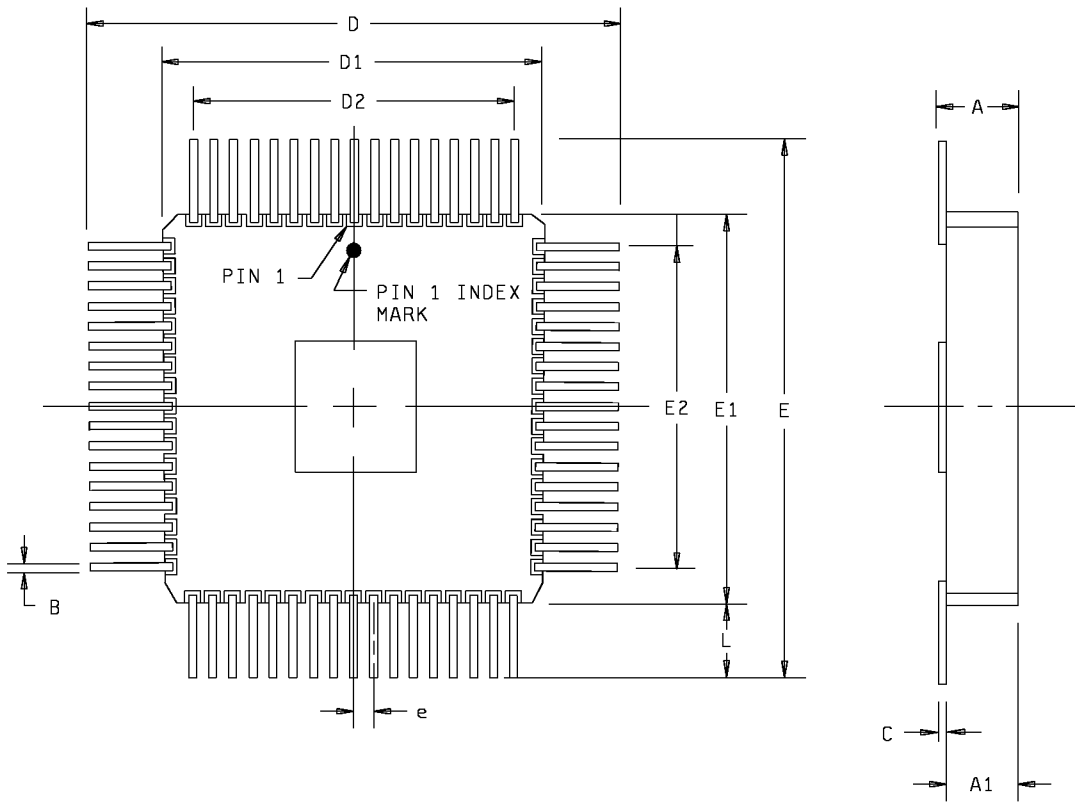
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{BUSY}$ disable time to address	t_{BDA}	See figures 5 and 8. 2/	9, 10, 11	01,03,05 07,09		45	ns
				11		40	
$\overline{BUSY}$ access time to chip enable	t_{BAC}	See figures 5 and 8. 2/	9, 10, 11	01,07 03,05, 09,11		35	ns
$\overline{BUSY}$ disable time to chip enable	t_{BDC}	See figures 5 and 8. 2/	9, 10, 11	01,07 03,05, 09,11		30	ns
Write pulse to data delay 10/	t_{WDD}	See figures 5 and 8. 2/	9, 10, 11	01-04, 07-10		90	ns
				05,06 11,12		80	
Write data valid to read data delay 10/	t_{DDD}	See figures 5 and 8. 2/	9, 10, 11	01,02, 07,08		90	ns
				03,04, 09,10		70	
				05,06, 11,12		55	
$\overline{BUSY}$ disable to valid data	t_{BDD}	See figures 5 and 8. 2/	9, 10, 11	All		11/	ns
Arbitration priority setup time	t_{APS}	See figures 5 and 8. 2/	9, 10, 11	01,07 03,05, 09,11	5		ns

1/ At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no address or control lines change.
2/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V and input pulse levels of 0.0 V to 3.0 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF (see figure 5).
3/ May not be tested, but shall be guaranteed to the limits specified in table I.
4/ Test conditions assume signal transition times of 5.0 ns or less. Transition is measured at steady-state high level of -500 mV or steady-state low level of +500 mV on the output from 1.5 V level on the input with a load capacitance of 5.0 pF (see figure 5).
5/ For master/slave combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$.
6/ Specified for $\overline{OE}$ at high.
7/ The specification for t_{DH} must be met by the device supplying write data to the RAM under all conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will be smaller than the actual t_{OW}.
8/ To ensure that the write cycle is inhibited during contention. Applicable to slave devices only (device types 02, 04, 06, 08, 10 and 12).
9/ To ensure that a write cycle is completed after contention. Applicable to slave devices only (device types 02, 04, 06, 08, 10, and 12).
10/ Port to port delay through RAM cells from writing port to reading port.
11/ t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual), or $t_{DDD} - t_{DW}$ (actual).

Case outline U

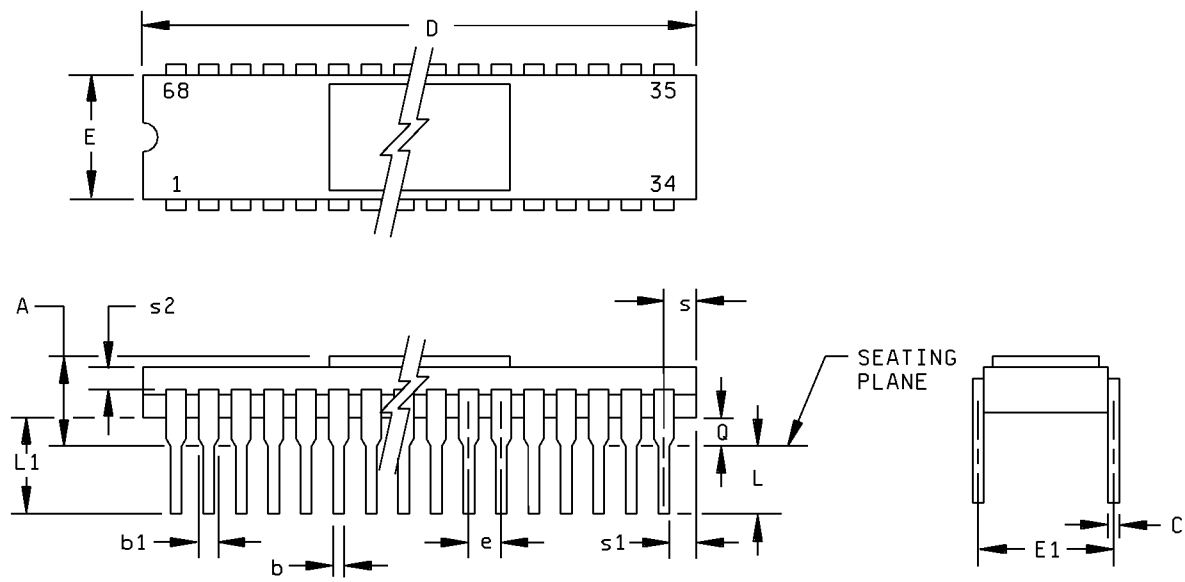


Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.080	.120	2.03	3.05	D2/E2	.800 BSC		20.32 BSC	
A1	.070	.090	1.78	2.29	e	.050 BSC		1.27 BSC	
B	.014	.021	0.36	0.53	L	.350	.450	8.89	11.43
C	.008	.012	0.20	0.30	N	68			
D/E	1.640	1.870	41.66	47.50	ND	17			
D1/E1	.926	.970	23.52	24.64					

NOTES:
1. All dimensions are in inches.
2. Metric equivalents are given for general information only.
3. BSC - Basic lead spacing between centers.
4. Symbol "N" represents number of leads.

FIGURE 1. Case outlines.

Case outline X



Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.085	.190	2.16	4.83	e	.070 BSC		1.78 BSC	
b	.014	.023	0.36	0.58	L	.125	.200	3.18	5.08
b1	.030	.060	0.76	1.52	L1	.150	---	3.81	---
C	.008	.015	0.20	0.38	Q	.020	.070	0.51	1.78
D	2.380	2.440	60.45	61.98	S	.030	.065	0.77	1.66
E	.580	.610	14.73	15.49	S1	.005	---	0.12	---
E1	.590	.620	14.99	15.75	S2	.005	---	0.12	---

FIGURE 1. Case outlines - Continued.

Device types	All	All	Device types	All	All
Case outlines	U, X, and Y	Z	Case outlines	U, X, and Y	Z
Terminal number	Terminal symbol 1/		Terminal number	Terminal symbol 1/	
1	I/O_{0L}	I/O_{9L}	35	GND 2/	A_{5R}
2	I/O_{1L}	I/O_{10L}	36	$R/\overline{W}_{RUB}$	A_{4R}
3	I/O_{2L}	I/O_{11L}	37	$R/\overline{W}_{RLB}$	A_{3R}
4	I/O_{3L}	I/O_{12L}	38	$\overline{OE}_R$	A_{2R}
5	I/O_{4L}	I/O_{13L}	39	A_{10R}	A_{1R}
6	I/O_{5L}	I/O_{14L}	40	A_{9R}	A_{0R}
7	I/O_{6L}	I/O_{15L}	41	A_{8R}	$\overline{BUSY}_R$
8	I/O_{7L}	V_{CC} 2/	42	A_{7R}	$\overline{CE}_R$
9	I/O_{8L}	GND 2/	43	A_{6R}	$\overline{CE}_L$
10	I/O_{9L}	I/O_{0R}	44	A_{5R}	$\overline{BUSY}_L$
11	I/O_{10L}	I/O_{1R}	45	A_{4R}	A_{0L}
12	I/O_{11L}	I/O_{2R}	46	A_{3R}	A_{1L}
13	I/O_{12L}	I/O_{3R}	47	A_{2R}	A_{2L}
14	I/O_{13L}	I/O_{4R}	48	A_{1R}	A_{3L}
15	I/O_{14L}	I/O_{5R}	49	A_{0R}	A_{4L}
16	I/O_{15L}	I/O_{6R}	50	$\overline{BUSY}_R$	A_{5L}
17	V_{CC} 2/	I/O_{7R}	51	$\overline{CE}_R$	A_{6L}
18	GND 2/	I/O_{8R}	52	$\overline{CE}_L$	A_{7L}
19	I/O_{0R}	I/O_{9R}	53	$\overline{BUSY}_L$	A_{8L}
20	I/O_{1R}	I/O_{10R}	54	A_{0L}	A_{9L}
21	I/O_{2R}	I/O_{11R}	55	A_{1L}	A_{10L}
22	I/O_{3R}	I/O_{12R}	56	A_{2L}	$\overline{OE}_L$
23	I/O_{4R}	I/O_{13R}	57	A_{3L}	$R/\overline{W}_{LLB}$
24	I/O_{5R}	I/O_{14R}	58	A_{4L}	$R/\overline{W}_{LUB}$
25	I/O_{6R}	I/O_{15R}	59	A_{5L}	V_{CC} 2/
26	I/O_{7R}	GND 2/	60	A_{6L}	I/O_{0L}
27	I/O_{8R}	$R/\overline{W}_{RUB}$	61	A_{7L}	I/O_{1L}
28	I/O_{9R}	$R/\overline{W}_{RLB}$	62	A_{8L}	I/O_{2L}
29	I/O_{10R}	$\overline{OE}_R$	63	A_{9L}	I/O_{3L}
30	I/O_{11R}	A_{10R}	64	A_{10L}	I/O_{4L}
31	I/O_{12R}	A_{9R}	65	$\overline{OE}_L$	I/O_{5L}
32	I/O_{13R}	A_{8R}	66	$R/\overline{W}_{LLB}$	I/O_{6L}
33	I/O_{14R}	A_{7R}	67	$R/\overline{W}_{LUB}$	I/O_{7L}
34	I/O_{15R}	A_{6R}	68	V_{CC} 2/	I/O_{8L}

1/ An "L" suffix on a terminal indicates it applies to the "left port", and an "R" suffix indicates it applies to the "right port".
2/ Both V_{CC} pins and both GND pins must be connected to the supply in order to assure reliable operation.

FIGURE 2. Terminal connections.

Noncontention read/write control for all device types 1/

Left or right port 2/						Function
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	
X	X	H	X	Z	Z	Port disabled and in power down mode, I_{SB2} or I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L$ = H, power down mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on lower byte and upper byte written into memory. 3/
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on lower byte written into memory.3/ Data in memory output on upper byte. 4/
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in memory output on lower byte. 4/ Data on upper byte written into memory.3/
L	H	L	H	$DATA_{IN}$	Z	Data on lower byte written in memory. 3/
H	L	L	H	Z	$DATA_{IN}$	Data on upper byte written into memory. 3/
H	H	L	L	$DATA_{OUT}$	DATAOUT	Data in memory output on lower byte and upper byte. 4/
H	H	L	H	Z	Z	High impedance outputs.

1/ H = High, Z = High impedance,
L = Low, LB = Lower byte,
X = Don't care, UB = Upper byte.

2/ $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$

3/ If $\overline{BUSY}$ = L, data is not written.

4/ If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.

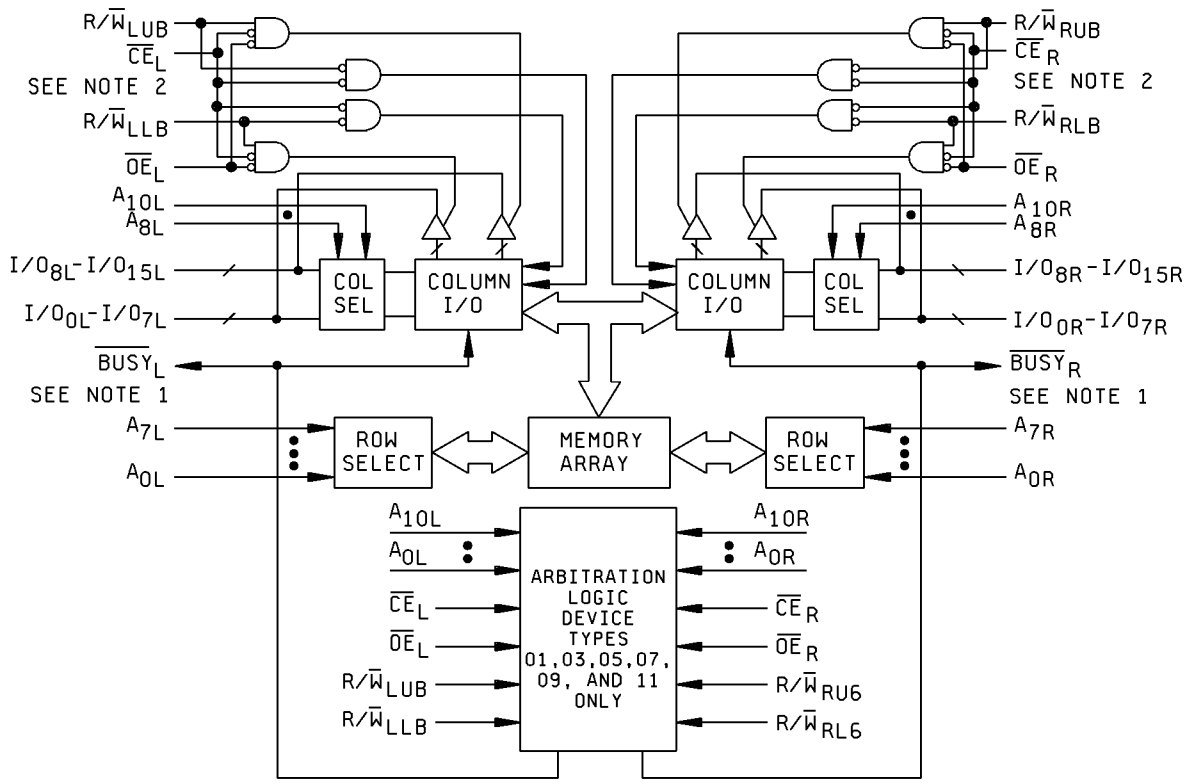
FIGURE 3. Truth tables.

Arbitration 1/

Left port		Right port		Flags		Function
$\overline{CE}_L$	A_{0L}-A_{10L}	$\overline{CE}_R$	A_{0R}-A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No contention
L	Any	H	X	H	H	No contention
H	X	L	Any	H	H	No contention
L	≠ A_{0R}-A_{10R}	L	≠ A_{0L}-A_{10L}	H	H	No contention
Address arbitration with $\overline{CE}$ low before address match						
L	LV5R	L	LV5R	H	L	L-Port wins
L	RV5L	L	RV5L	L	H	R-Port wins
L	Same	L	Same	H	L	Arbitration resolved
L	Same	L	Same	L	H	Arbitration resolved
$\overline{CE}$ arbitration with address match before $\overline{CE}$						
LL5R	=A_{0R}-A_{10R}	LL5R	=A_{0L}-A_{10L}	H	L	L-Port wins
RL5L	= A_{0R}-A_{10R}	RL5L	= A_{0L}-A_{10L}	L	H	R-Port wins
LW5R	= A_{0R}-A_{10R}	LW5R	= A_{0L}-A_{10L}	H	L	Arbitration resolved
LW5R	= A_{0R}-A_{10R}	LW5R	= A_{0L}-A_{10L}	L	H	Arbitration resolved

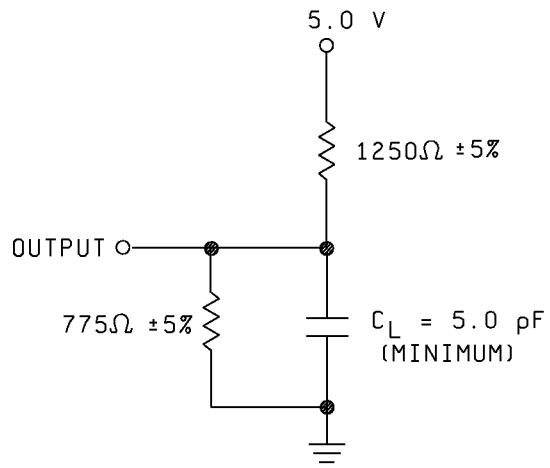
1/ X = Don't care,
L = Low,
H = High,
LV5R = Left address valid ≥ 5 ns before right address,
RV5L = Right address valid ≥ 5 ns before left address,
Same = Left and right address match within 5 ns of each other,
LL5R = Left $\overline{CE}$ = Low ≥ 5 ns before right $\overline{CE}$,
RL5L = Right $\overline{CE}$ = Low ≥ 5 ns before left $\overline{CE}$,
LW5R = Left and right $\overline{CE}$ = Low within 5 ns of each other.

FIGURE 3. Truth tables - Continued.

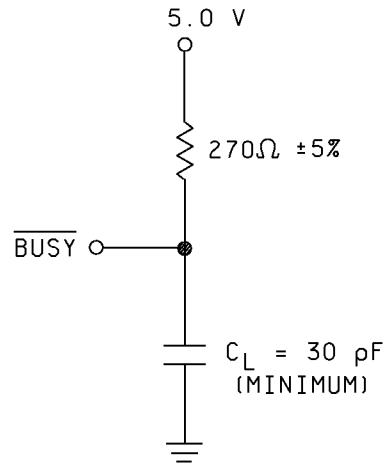


NOTES:
1. On device types 01, 03, 05, 07, 09, and 11, $\overline{\text{BUSY}}$ is an open drain output and requires the use of a pull-up resistor. On device types 02, 04, 06, 08, 10, and 12 $\overline{\text{BUSY}}$ is an input.
2. An "L" suffix on a terminal indicates it applies to the "left port", and "R" suffix indicates it applies to the "right port". "UB" indicates "upper byte" and an "LB" indicates "lower byte".

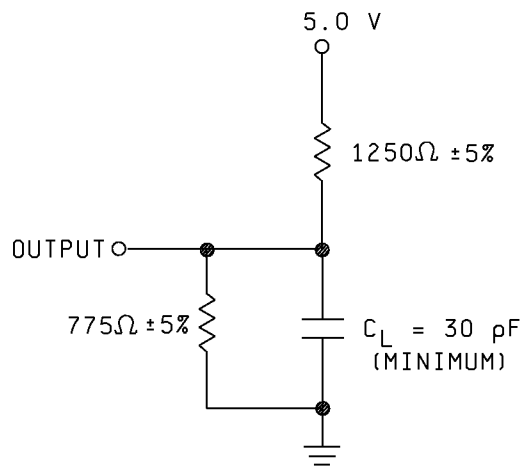
FIGURE 4. Block diagram.



OUTPUT LOAD CIRCUIT
FOR t_{HZ}, t_{LZ}, t_{WZ},
AND t_{OW}



OUTPUT LOAD CIRCUIT
FOR BUSY OUTPUT.
(APPLIES TO DEVICE
TYPES 01, 03, 05,
07, 09, AND 11 ONLY)

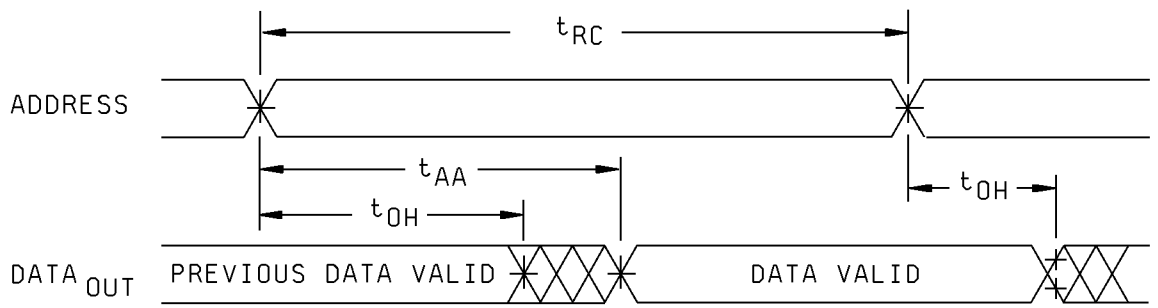


OUTPUT LOAD CIRCUIT
FOR ALL OTHER MEASUREMENTS

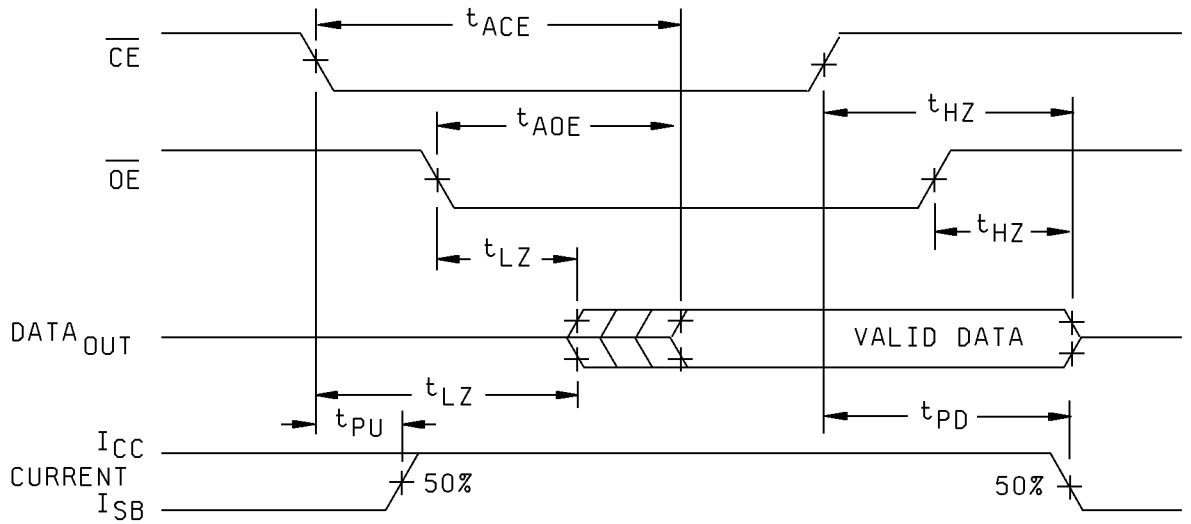
NOTE: C_L = Load capacitance and includes scope and jig capacitance.

FIGURE 5. Output load circuits.

READ CYCLE 1 - EITHER SIDE: SEE NOTES 1, 2, AND 4



READ CYCLE 2 - EITHER SIDE: SEE NOTES 1 AND 3



NOTES:
1. R/W is high for read cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.

FIGURE 6. Read cycle timing diagrams.

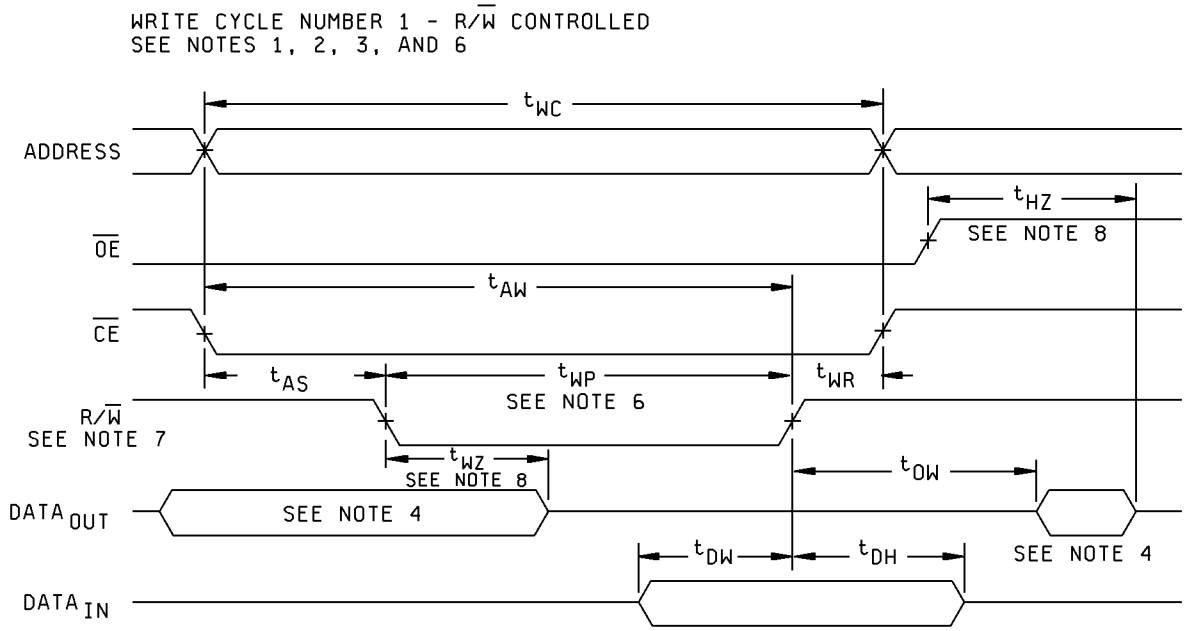
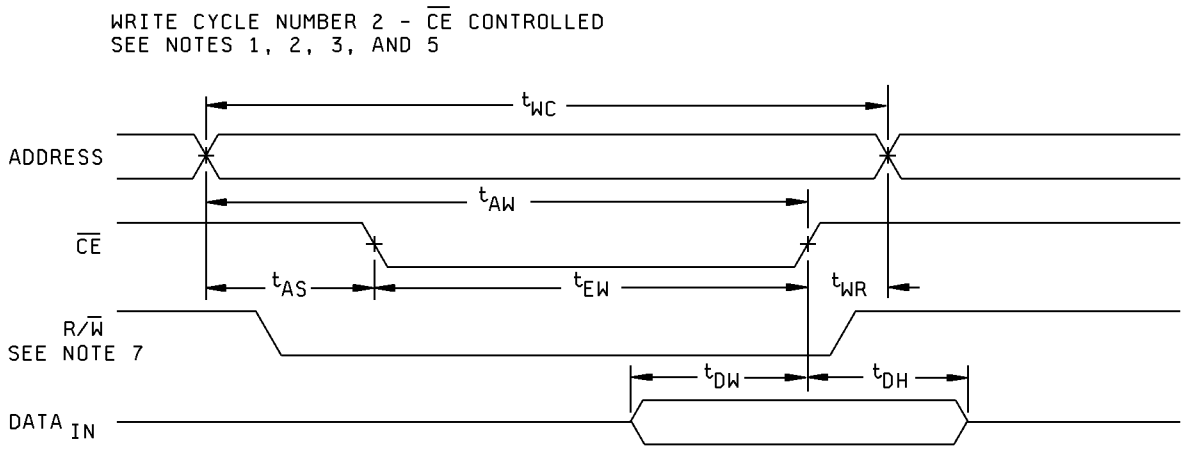


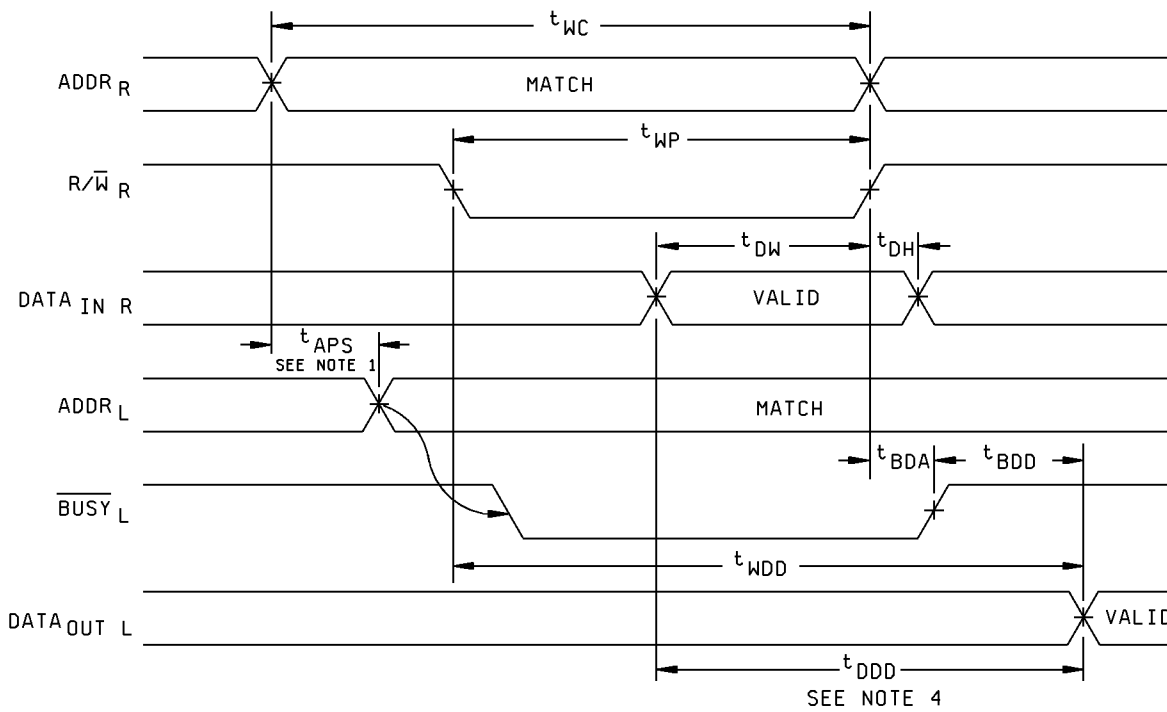
FIGURE 7. Write cycle timing diagrams.



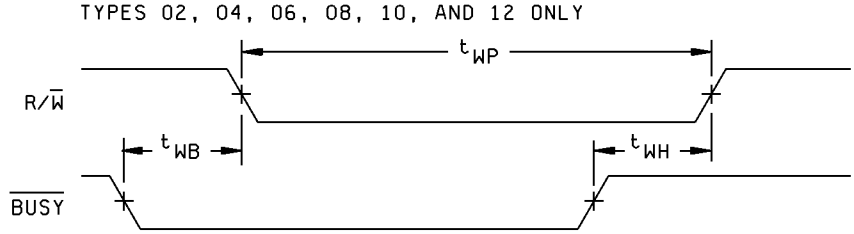
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
7. R/$\overline{W}$ for either upper or lower byte.
8. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig).

FIGURE 7. Write cycle timing diagrams - Continued.

READ WITH $\overline{\text{BUSY}}$ CYCLE FOR DEVICE TYPES 01, 03, 05, 07, 09, AND 11 ONLY. SEE NOTES 1, 2, AND 3



WRITE WITH $\overline{\text{BUSY}}$ CYCLE FOR DEVICE TYPES 02, 04, 06, 08, 10, AND 12 ONLY



NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. $\overline{\text{CE}}$ is continuously enabled for both ports.
4. $\overline{\text{OE}}$ at low for the reading port.

FIGURE 8. $\overline{\text{BUSY}}$ timing diagrams.

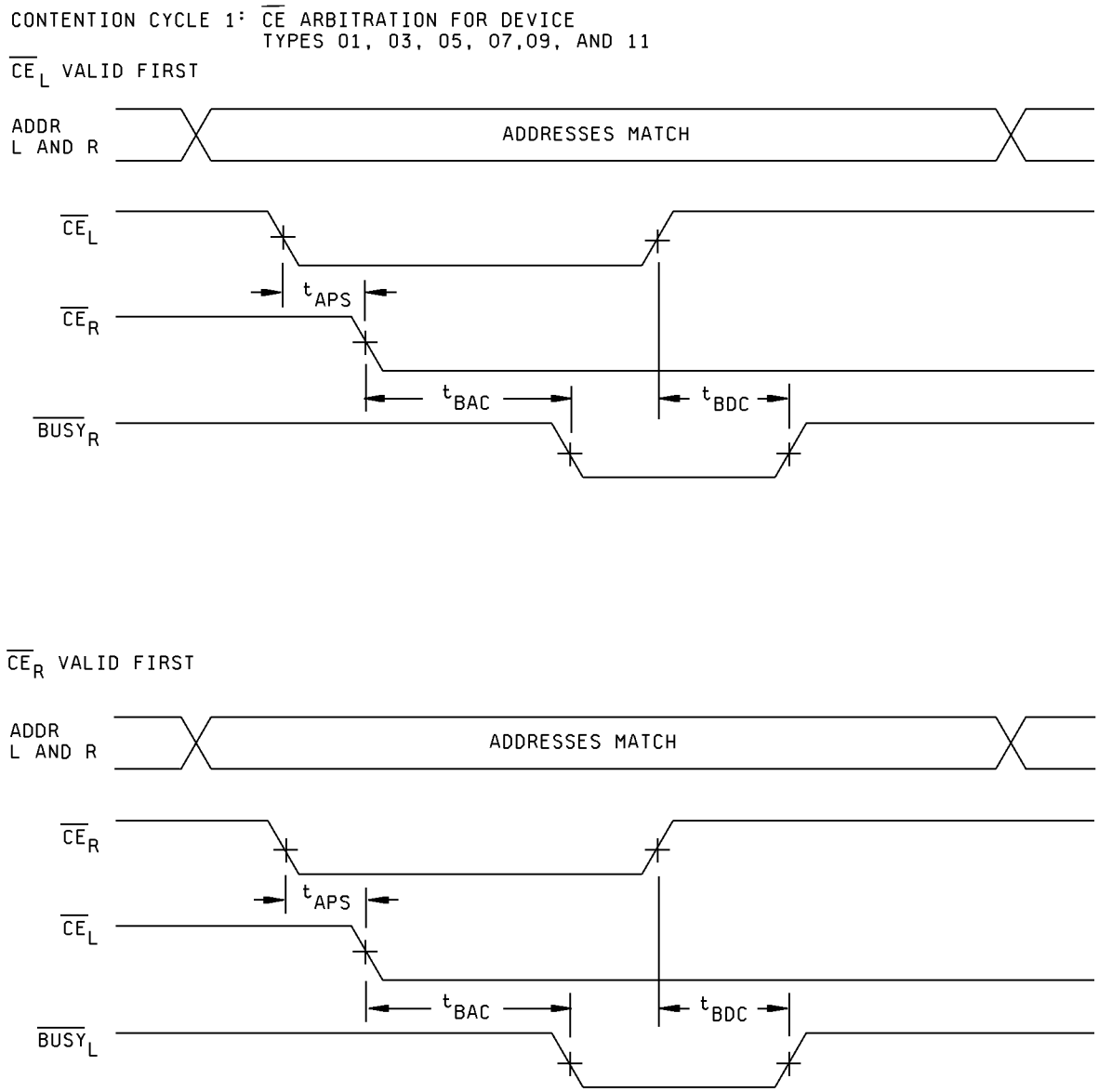
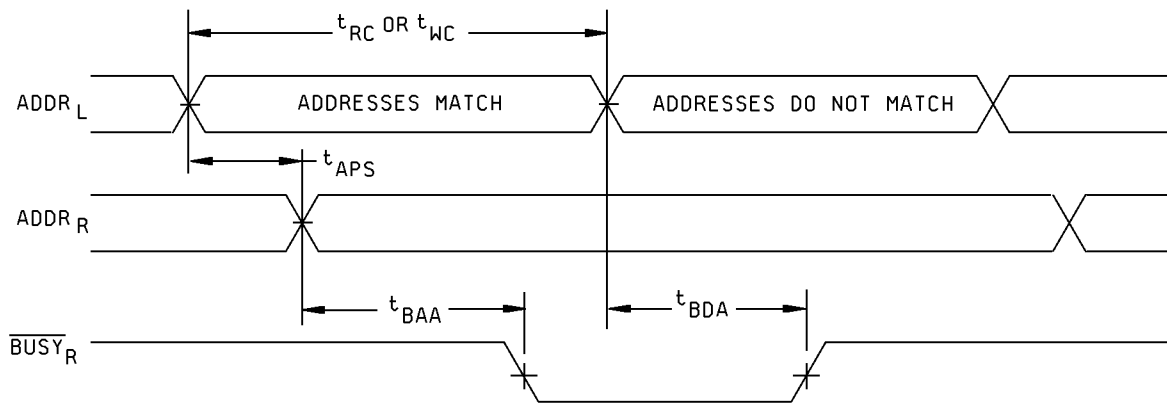


FIGURE 8. BUSY timing diagrams - Continued.

CONTENTION CYCLE 2: ADDRESS VALID ARBITRATION ($\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}
FOR DEVICE TYPES 01, 03, 05, 07, 09, AND 11)

LEFT ADDRESS VALID FIRST



RIGHT ADDRESS VALID FIRST

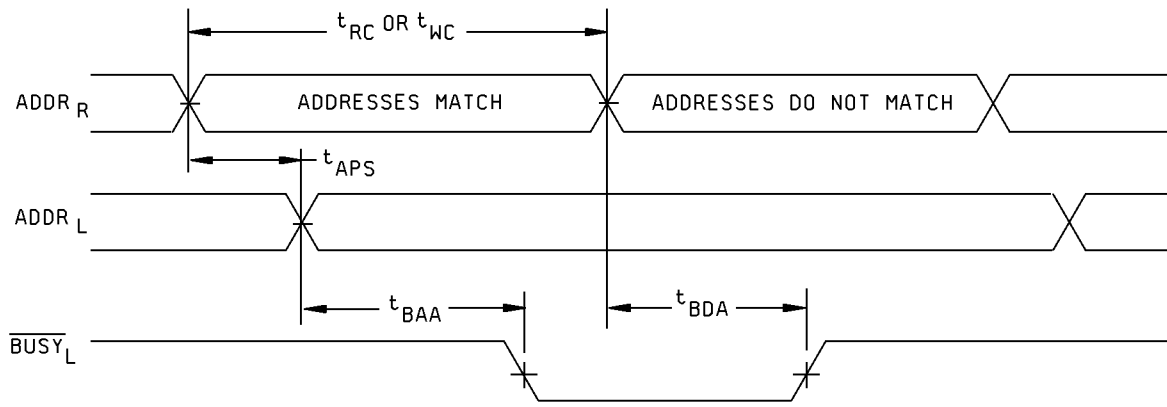


FIGURE 8. $\overline{BUSY}$ timing diagrams - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A, 8B,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8A, 8B,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1c

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualifcation and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-12-01

Approved sources of supply for SMD 5962-89712 are listed below for immediate acquisition only and shall be added to QML-38535 and MIL-HDBK-103 during the next revision. QML-38535 and MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38535 and MIL-HDBK-103.

Standard microcircuit drawing part number 1/	Vendor CAGE number	Vendor similar part number 3/
5962-8861001UA	2/	IDT7133S90FB
5962-8861001XA	2/	IDT7133S90XCB
5962-8861001YA	2/	IDT7133S90L68B
5962-8861001ZA	2/	IDT7133S90GB
5962-8861002UA	2/	IDT7143S90FB
5962-8861002XA	2/	IDT7143S90XCB
5962-8861002YA	2/	IDT7143S90L68B
5962-8861002ZA	2/	IDT7143S90GB
5962-8861003UA	2/	IDT7133SA70FB
5962-8861003XA	2/	IDT7133SA70XCB
5962-8861003YA	2/	IDT7133SAL68B
5962-8861003ZA	2/	IDT7133SA70GB
5962-8861004UA	2/	IDT7143S70FB
5962-8861004XA	2/	IDT7143S70XCB
5962-8861004YA	2/	IDT7143S70L68B
5962-8861004ZA	2/	IDT7143S70GB
5962-8861005UA	2/	IDT7133SA55FB
5962-8861005XA	2/	IDT7133SA55XCB
5962-8861005YA	2/	IDT7133SA55L68B
5962-8861005ZA	2/	IDT7133SA55GB
5962-8861006UA	2/	IDT7143S55FB
5962-8861006XA	2/	IDT7143S55XCB
5962-8861006YA	2/	IDT7143S55L68B
5962-8861006ZA	2/	IDT7143S55GB
5962-8861007UA	61772	IDT7133SA90FB
5962-8861007ZA	61772	IDT7133SA90GB
5962-8861008UA	61772	IDT7143SA90FB
5962-8861008ZA	61772	IDT7143SA90GB
5962-8861009UA	61772	IDT7133SA70FB
5962-8861009ZA	61772	IDT7133SA70GB
5962-8861010UA	61772	IDT7143SA70FB
5962-8861010ZA	61772	IDT7143SA70GB
5962-8861011UA	61772	IDT7133SA55FB
5962-8861011ZA	61772	IDT7133SA55GB
5962-8861012UA	61772	IDT7143SA55FB
5962-8861012ZA	61772	IDT7143SA55GB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Not available from an approved source of supply.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 2975 Stender Way Santa Clara, CA 95054-8015

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.