REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-02-23

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-96773

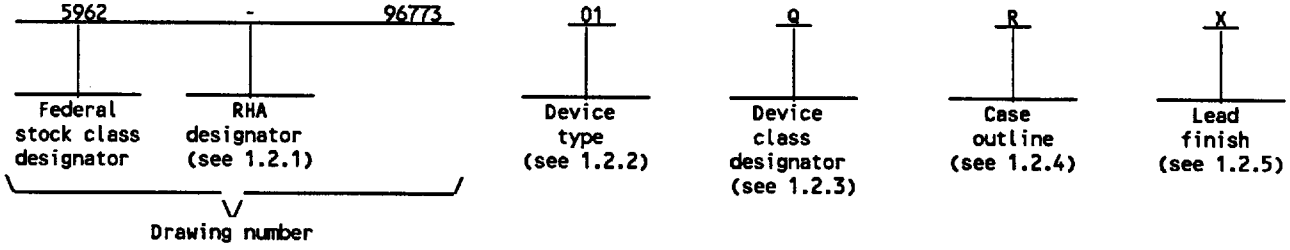
SHEET 1 OF 14

DESC FORM 193
JUL 94

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC574	Octal edge-triggered D-type flip-flop with three-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} +0.5 V dc 4/
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V or V_{IN} > V_{CC})	±20 mA
DC output clamp current (I_{OK})(V_{IN} < 0.0 V or V_{OUT} > V_{CC})	±20 mA
Continuous output current (I_O) (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Minimum high level input voltage (V_{IH}):	
V_{CC} = 3.0 V	+2.1 V
V_{CC} = 4.5 V	+3.15 V
V_{CC} = 5.5 V	+3.85 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 3.0 V	+0.9 V
V_{CC} = 4.5 V	+1.35 V
V_{CC} = 5.5 V	+1.65 V
Maximum high level output current (I_{OH}):	
V_{CC} = 3.0 V	-12 mA
V_{CC} = 4.5 V	-24 mA
V_{CC} = 5.5 V	-24 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 3.0 V	+12 mA
V_{CC} = 4.5 V	+24 mA
V_{CC} = 5.5 V	+24 mA
Input rise or fall time rate ($\Delta t/\Delta V$)	0 to 8 ns/V
case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C. Unused inputs must be held high or low.
4/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.
5/ Values will be added when they become available.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$, $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test $V_{IN} = V_{IL}$ or V_{IH} For all other inputs $V_{IN} = V_{CC}$ or GND	$I_{OH} = -50\ \mu A$	3.0 V	1, 2, 3	2.9		V
				4.5 V		4.4		
				5.5 V		5.4		
	V_{OH2}		$I_{OH} = -12$ mA	3.0 V	1	2.56		
					2, 3	2.4		
	V_{OH3}		$I_{OH} = -24$ mA	4.5 V	1	3.94		
					2, 3	3.7		
				5.5 V	1	4.94		
					2, 3	4.7		
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test $V_{IN} = V_{IL}$ or V_{IH} For all other inputs $V_{IN} = V_{CC}$ or GND	$I_{OL} = 50\ \mu A$	3.0 V	1, 2, 3		0.1	V
				4.5 V			0.1	
				5.5 V			0.1	
	V_{OL2}		$I_{OL} = 12$ mA	3.0 V	1		0.36	
					2, 3		0.5	
	V_{OL3}		$I_{OL} = 24$ mA	4.5 V	1		0.36	
					2, 3		0.5	
				5.5 V	1		0.36	
					2, 3		0.5	
Input current high 3010	I_{IH}	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		5.5 V	1		+0.1	µA
					2, 3		+1.0	
Input current low 3009	I_{IL}	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		5.5 V	1		-0.1	µA
					2, 3		-1.0	
Three-state output leakage current high 3021	I_{OZH}	$\overline{OE} = V_{IH}$ For all other inputs, $V_{IN} = V_{CC}$ or GND $V_{OUT} = V_{CC}$		5.5 V	1		+0.5	µA
					2, 3		+5.0	
Three-state output leakage current low 3021	I_{OZL}	$\overline{OE} = V_{IH}$ For all other inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = GND		5.5 V	1		-0.5	µA
					2, 3		-5.0	
Quiescent supply current 3005	I_{CC}	For all inputs, $V_{IN} = V_{CC}$ or GND I_{OUT} = 0 A		5.5 V	1		4.0	µA
					2, 3		80.0	
Power dissipation capacitance	C_{PD} 4/	T_C = +25°C, See 4.4.1c		5.0 V	4		30	pF
Input capacitance 3012	C_{IN}	T_C = +25°C, $V_{IN} = V_{CC}$ or GND See 4.4.1c		5.0 V	4		9	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Functional test 3014	5/	For all inputs, $V_{IN} = V_{IH}$ or V_{IL} Verify output V_O See 4.4.1b	3.0 V	7, 8	L	H	
			4.5 V	7, 8	L	H	
			5.5 V	7, 8	L	H	
Pulse duration, CLK high or low	t_w	C_L = 50 pF minimum R_L = 500Ω See figure 4	3.0 V and 3.6 V	9	6.0		ns
				10, 11	4.5		
			4.5 V and 5.5 V	9	4.0		ns
				10, 11	5.0		
Setup time, high or low, data before CLK↑	t_s	C_L = 50 pF minimum R_L = 500Ω See figure 4	3.0 V and 3.6 V	9	2.5		ns
				10, 11	6.5		
			4.5 V and 5.5 V	9	1.5		ns
				10, 11	3.5		
Hold time, high or low, data after CLK↑	t_h	C_L = 50 pF minimum R_L = 500Ω See figure 4	3.0 V and 3.6 V	9	1.5		ns
				10, 11	2.5		
			4.5 V and 5.5 V	9	1.5		ns
				10, 11	2.5		
Maximum operating frequency	f_{MAX}	C_L = 50 pF mimimum R_L = 500Ω See figure 4	3.0 V and 3.6 V	9	75		MHz
				10, 11	55		
			4.5 V and 5.5 V	9	95		
				10, 11	85		
Propagation delay time, CLK to mQ 3003	t_{PLH} 6/	C_L = 50 pF minimum R_L = 500Ω See figure 4	3.0 V and 3.6 V	9	3.5	13.5	ns
				10, 11	1.0	16.5	
			4.5 V and 5.5 V	9	2.0	9.5	ns
				10, 11	1.5	11.5	
	t_{PHL} 6/		3.0 V and 3.6 V	9	3.5	12.0	ns
				10, 11	1.0	15.0	
			4.5 V and 5.5 V	9	2.0	8.5	ns
				10, 11	1.5	10.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Propagation delay time, output enable, $\overline{OE}$ to mQ 3003	t_{PZH} 6/	C_L = 50 pF minimum R_L = 500Ω See figure 4	3.0 V and 3.6 V	9	2.5	11.0	ns
				10, 11	1.0	13.0	
			4.5 V and 5.5 V	9	2.0	8.5	ns
				10, 11	1.5	9.5	
	t_{PZL} 6/		3.0 V and 3.6 V	9	3.0	10.5	ns
				10, 11	1.0	12.5	
			4.5 V and 5.5 V	9	2.0	8.0	ns
				10, 11	1.5	9.5	
Propagation delay time, output disable, $\overline{OE}$ to mQ 3003	t_{PHZ} 6/	C_L = 50 pF minimum R_L = 500Ω See figure 4	3.0 V and 3.6 V	9	3.5	12.0	ns
				10, 11	1.0	14.0	
			4.5 V and 5.5 V	9	2.0	9.5	ns
				10, 11	1.5	11.5	
	t_{PLZ} 6/		3.0 V and 3.6 V	9	2.0	9.0	ns
				10, 11	1.0	10.5	
			4.5 V and 5.5 V	9	1.0	7.5	ns
				10, 11	1.5	9.0	

1/ For tests not listed in the referenced MIL-STD-883, utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. The values to be used for V_{IH} and V_{IL} shall be the V_{IH} minimum and V_{IL} maximum values listed in section 1.4 herein.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

4/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). where

$$P_D = (C_{PD} + C_L)(V_{CC} \times I_{CC})f + (I_{CC} \times V_{CC})$$
$$I_S = (C_{PD} + C_L)\ V_{CC} f + I_{CC}$$

f is the frequency of the input signal and C_L is external output load capacitance.

5/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883 may be incorporated. For outputs, $L < 0.3V_{CC}$ and $H \ge 0.7V_{CC}$.

6/ For propagation delay tests, all paths must be tested.

Device type	01
Case outlines	R, S, 2
Terminal number	Terminal symbol
1	$\overline{OE}$
2	1D
3	2D
4	3D
5	4D
6	5D
7	6D
8	7D
9	8D
10	GND
11	CLK
12	8Q
13	7Q
14	6Q
15	5Q
16	4Q
17	3Q
18	2Q
19	1Q
20	V_{CC}

Pin description	
Terminal symbol	Description
mD (m = 1 to 8)	Data inputs
mQ (m = 1 to 8)	Data outputs
$\overline{OE}$	Output enable control input
CLK	Clock

FIGURE 1. Terminal connections.

Inputs			Outputs
$\overline{OE}$	CLK	mD	mQ
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = Disabled
↑ = Low-to-high transition of clock.
Q_0 = The level of Q before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

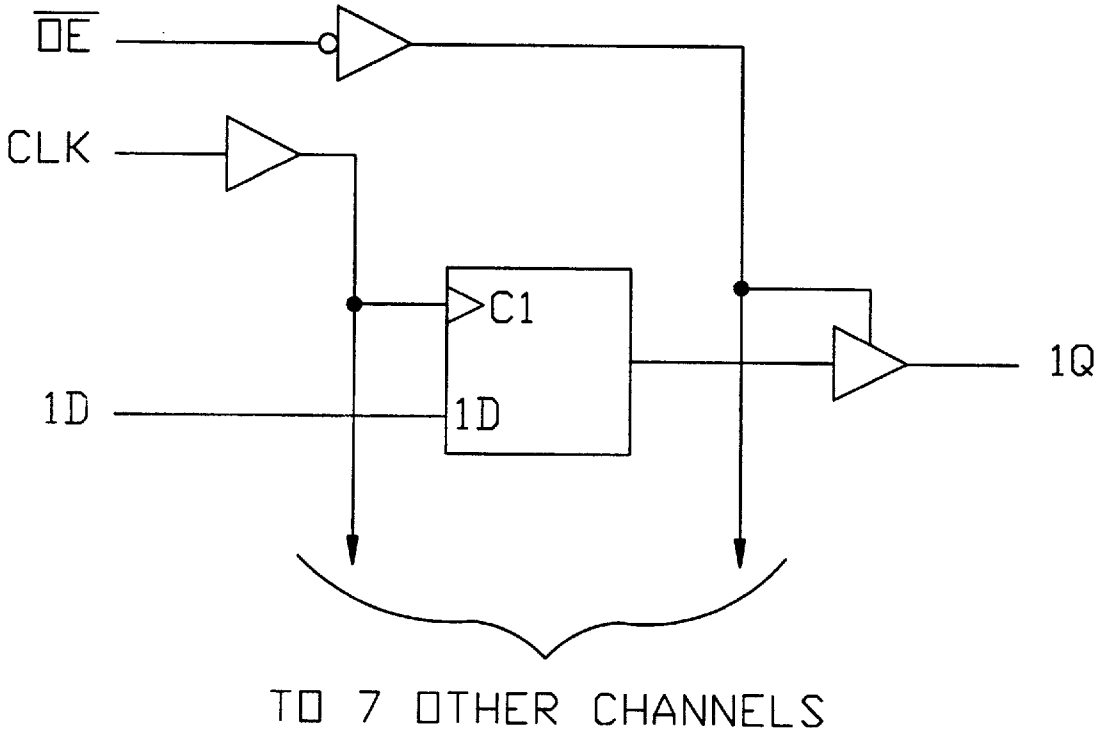


FIGURE 3. Logic diagram.

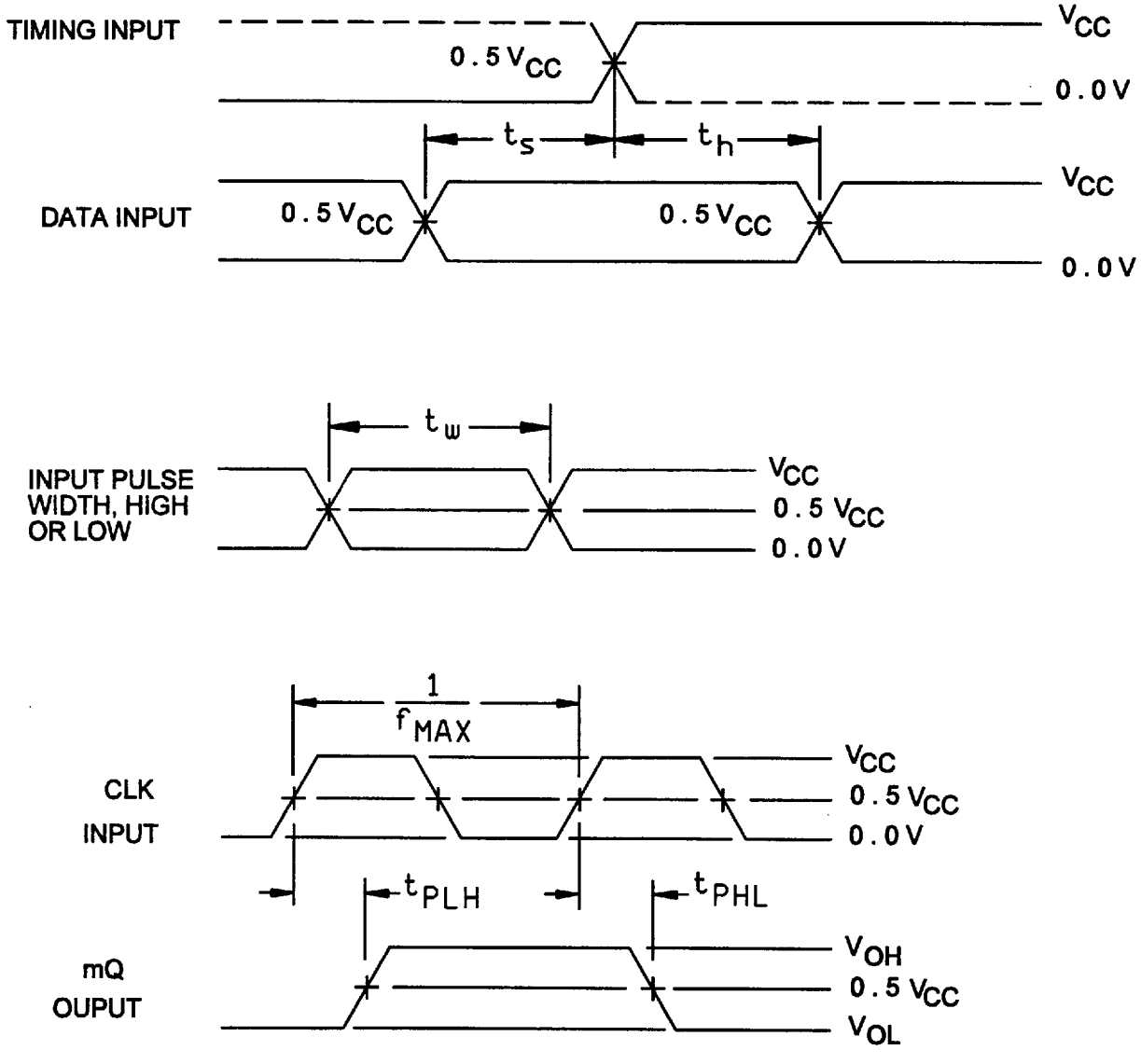
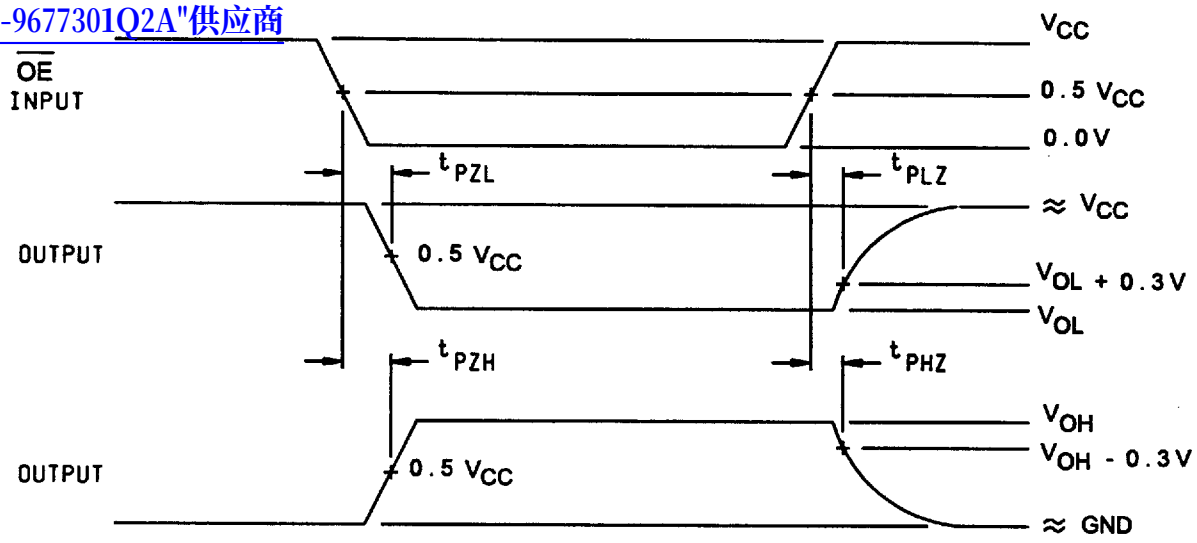
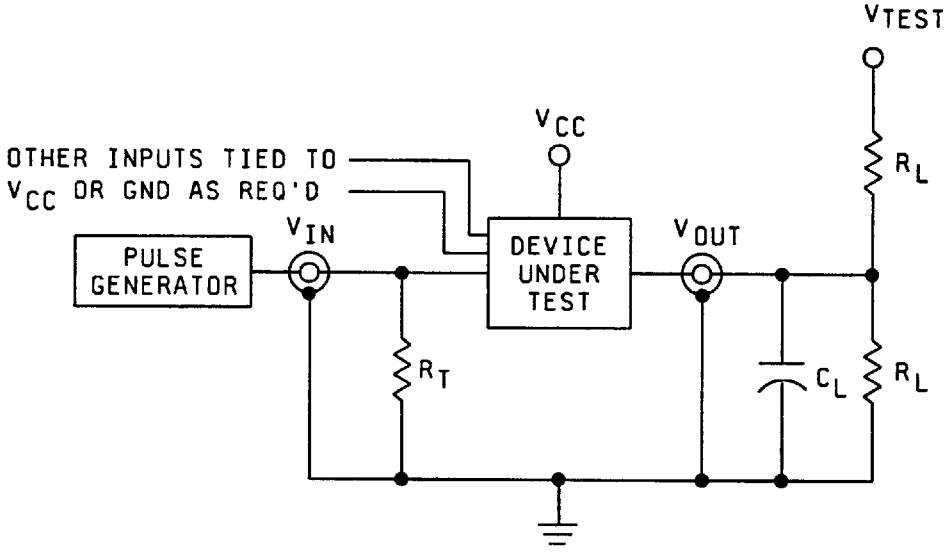


FIGURE 4. Switching waveforms and test circuit.





NOTES:
1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 x V_{CC}
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3V_{CC} to 0.7V_{CC} and from 0.7V_{CC} to 0.3V_{CC}, respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{PD} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The QM plan shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.