17 ELECTRICAL SPECIFICATIONS

Table 17-1: 65550 Absolute Maximum Conditions

Symbol	Parameter	Min	Typical	Max	Units
P_D	Power Dissipation	—	—	3.0	W
V_{CC}	Supply Voltage†	-0.5	—	7.0	V
V_I	Input Voltage	-0.5	—	V_{CC} +0.5	V
V_O	Output Voltage	-0.5	—	V_{CC} +0.5	V
T_{OP}	Operating Temp	-25	—	85	°C
T_{STG}	Storage Temp	-40	—	125	°C

Note: Permanent device damage may occur if Absolute Maximum Rating are exceeded.
Functional operation must be restricted to the conditions under Normal Operating Conditions.

Table 17-2: 65550 Normal Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units
V_{CC5}	Supply Voltage†	4.5	5.0	5.5	V
V_{CC33}	Supply Voltage†	3.0	3.3	3.6	V
T_A	Ambient Temperature	0	—	70	°C

Table 17-3: 65550 DAC Characteristics
(Under Normal Operating Condtions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typical	Max	Units
V_O	Output Voltage	IO ≤ 10 mA	1.5	–	–	V
I_O	Output Current	VO ≤ 1V @ 37.5Ω Load	21	–	–	mA
	Full Scale Error		–	–	± 5	%
	DAC to DAC Correlation		–	1.27	–	%
	DAC Linearity		± 2	–	–	LSB
	Glitch Energy		–	–	200	pVsec
	Comparator Sensitivity		–	50	–	mV

Note:
† IVCC and CVCC must ALWAYS be tied to the same voltage supply, and AVCC must NEVER be provided with a voltage supply that is higher than IVCC and CVCC.

Table 17- 4: 65550 DC Characteristics
(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typical	Max	Units
P_{D33}	Power Dissipation	All VCCs at 3.3V	–	–	1.5	W
P_{D50}	Power Dissipation	All VCCs at 5.0V	–	–	2.5	W
I_{CCE5}	Power Supply Current	0°C, 5.5V, MCLK=40 MHz, DAC on ††	–	TBD	TBD	mA
I_{CCO5}	Power Supply Current	0°C, 5.5V, MCLK=40 MHz, DAC off ††	–	TBD	TBD	mA
I_{CCE3}	Power Supply Current	0°C, 3.3V, MCLK=40 MHz, DAC on ††	–	TBD	TBD	mA
I_{CCO3}	Power Supply Current	0°C, 3.3V, MCLK=40 MHz, DAC off ††	–	TBD	TBD	mA
I_{CCSD}	Power Supply Current	0°C, 3.3V, Standby, Self Refresh DRAMs†	–	TBD	TBD	µA
I_{CCSS}	Power Supply Current	0°C, 3.3V, Standby, SlowRfsh 32KHz in	–	TBD	TBD	µA
I_{CCSR}	Power Supply Current	0°C, 3.3V, Standby, SlowRfsh XTALI in	–	TBD	TBD	µA
I_{IL}	Input Leakage Current		–100	–	+100	µA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	µA
V_{IL}	Input Low Voltage	All input pins	–0.5	–	0.8	V
V_{IH}	Input High Voltage	All input pins	2.0	–	VCC+0.5	V
V_{THR}	Input Switch Point	All inputs except RESET# & STNDBY#	–	1.4	–	V
V_{HYS}	Input Hysteresis	RESET# and STNDBY#	–	± 0.15	–	V
V_{OL5}	Output Low Voltage	Under max load per table 17-5 (5V)	–	–	0.5	V
V_{OL3}	Output Low Voltage	Under max load per table 17-5 (3.3V)	–	–	0.5	V
V_{OH5}	Output High Voltage	Under max load per table 17-5 (5V)	2.4	–	–	V
V_{OH3}	Output High Voltage	Under max load per table 17-5 (3.3V)	0.7xVcc	–	–	V

Notes:
† Measured with all chip inputs driven to inactive levels and outputs not connected (or connected to typical external loads).
†† 640x480x8bpp, TFT panel (for power data regarding other configurations, contact Chips and Technobgies, Inc.).

Table 17- 5: 65550 DC Drive Characteristics
(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	AA0-AA9 H/VSYNC, P0-P23, SHFCLK, M	$V_{OUT}=V_{OL}$, see note†	12	mA
		DEVSEL#, PAR, PERR#, SERR#, STOP#, TRDY# CASAH/L#, CASBH/L#, CASCH/L#, CASDH/L# ACTI, D0-D31, ENABKL, ENAVDD, ENAVEE, FLM, LP	$V_{OUT}=V_{OL}$, see note†	8	mA
		COE#, RAS0#, RAS1#, WEA#, WEB#, WEC#, WED#	$V_{OUT}=V_{OL}$, see note†	4	mA
		All other outputs	$V_{OUT}=V_{OL}$, see note†	2	mA
I_{OH}	Output High Drive	AA0-AA9 H/VSYNC, P0-P23, SHFCLK, M	$V_{OUT}=V_{OL}$, see note†	12	mA
		DEVSEL#, PAR, PERR#, SERR#, STOP#, TRDY# CASAH/L#, CASBH/L#, CASCH/L#, CASDH/L# ACTI, D0-D31, ENABKL, ENAVDD, ENAVEE, FLM, LP	$V_{OUT}=V_{OL}$, see note†	8	mA
		COE#, RAS0#, RAS1#, WEA#, WEB#, WEC#, WED#	$V_{OUT}=V_{OL}$, see note†	4	mA
		All other outputs	$V_{OUT}=V_{OL}$, see note†	2	mA

Note: †IOL & IOH drive listed above indicates 5V low drive (Vcc=4.5V) and 3.3V high drive (Vcc=3V), as programmed.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

Table 17- 6: 65550 AC Test Conditions
(Under Normal Operating Condtions Unless Noted Otherwise)

Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
All 12mA, 8mA, 4mA outputs plus PAR for PCI	V_{OL}	2.4V	85pF
All Other 2mA output pads	V_{OL}	2.4V	40pF

Table 17- 7: 65550 AC Timing Characteristics - Reference Clock

Symbol	Parameter	Notes	Min	Typical	Max	Units
F_{REF}	Reference Frequency	(±100 ppm)	1	14.31818	60	MHz
T_{REF}	Reference Clock Period	$1/F_{REF}$	16.6	69.84128	1000	nS
T_{HI}/T_{REF}	Reference Clock Duty Cycle		25	–	75	%

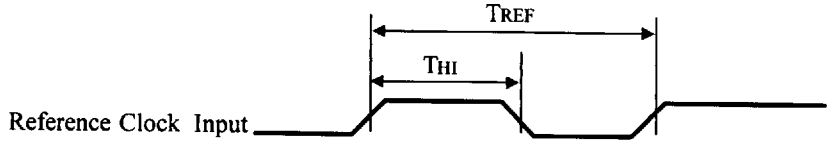


Figure 17-1: Reference Clock Timing

Table 17- 8: 65550 AC Timing Characteristics - Clock Generator

Symbol	Parameter	Notes	Min	Typical	Max	Units
T_C	DCLK Frequency (3.3V)-- 550A1		–	–	80	MHz
	DCLK Frequency (5.0V) -- 550A1 and 550A1-5		–	–	100	MHz
T_C	DCLK Frequency (3.3V)-- 550B		–	–	95	MHz
T_{CH}	DCLK High -- 550A1		TBD	–	TBD	
T_{CL}	DCLK Low -- 550A1		TBD	–	TBD	
T_{CH}	DCLK High -- 550B		TBD	–	TBD	
T_{CL}	DCLK Low -- 550B		TBD	–	TBD	
T_M	MCLK Frequency (3.3V)-- 550A1		–	–	38	MHz
	MCLK Frequency (5.0V) -- 550A1 and 550A1-5		–	–	38	MHz
T_M	MCLK Frequency (3.3V)-- 550B		–	–	50	MHz
T_{MH}	MCLK High -- 550A1 and 550A1-5		TBD	–	TBD	
T_{ML}	MCLK Low -- 550A1 and 550A1-5		TBD	–	TBD	
T_{MH}	MCLK High -- 550B		TBD	–	TBD	
T_{ML}	MCLK Low -- 550B		TBD	–	TBD	

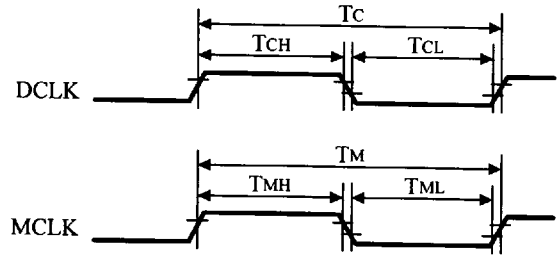


Figure 17-2: Clock Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

Table 17- 9: 65550 AC Timing Characteristics - Reset

Symbol	Parameter	Notes	Min	Max	Units
T_{IPR}	Reset Active Time from Power Stable	See Note 1	5	–	mS
T_{ORS}	Reset Active Time from Ext. Osc. Stable		0	–	mS
T_{RES}	Reset Active Time with Power Stable	See Note 2	2	–	mS
T_{STR}	Reset Active Time from Standby	RESET# is ignored in Standby Mode	2	–	mS
T_{RSR}	Reset Rise Time	Reset fall time is non-critical	–	20	nS
T_{RSO}	Reset Active to Output Float Delay		–	40	nS
T_{CSU}	Configuration Setup Time	See Note 3	20	–	nS
T_{CHD}	Configuration Hold Time		5	–	nS

Note 1: This parameter includes time for internal voltage stabil ization of all sections of the chip, startup and stabilization of the internal clock synthesizer, and setting of all internal logic to a known state.

Note 2: This parameter includes time for the internal clock synthe sizer to reset to its default frequency and time to set all internal logic to a known state. It assumes power is stable and the internal clock synthesizer is already operating at some stable frequency.

Note 3: This parameter specifies the setup time to latch reliably the state of the config uration bits. Changes in some configuration bits may take longer to stabilize inside the chip (such as internal clock synthe - sizer-related bits 4 and 5). The r ecommended configuration bit setup time is T_{RES} (2mS) to insure that the chip is in a completely stable state when Reset goes inactive.

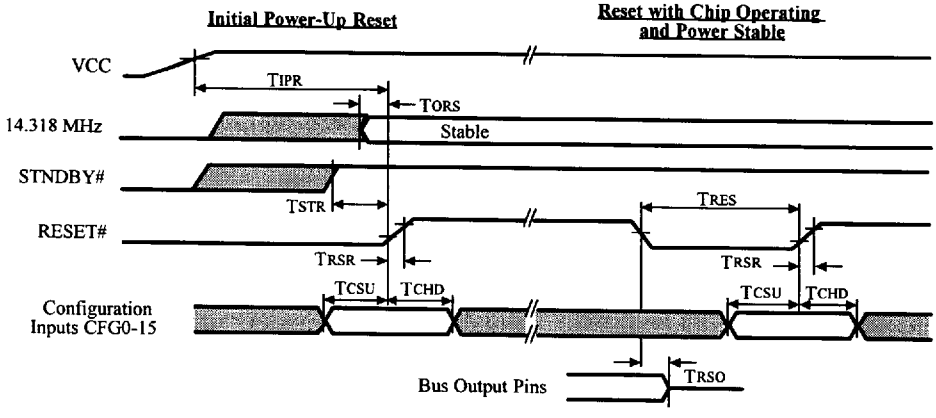


Figure 17-3: Reset Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

Table 17- 10: 65550 AC Timing Characteristics - PCI Bus Frame(33 MHz)

Symbol	Parameter	Notes	Min	Max	Units
T_{FRS}	FRAME# Setup to CLK		7	–	nS
T_{CMS}	C/BE#[3:0] (Bus CMD) Setup to CLK		7	–	nS
T_{CMH}	C/BE#[31:0] (Bus CMD) Hold from CLK		2	–	nS
T_{BES}	C/BE#[3:0] (Byte Enable) Setup to CLK		7	–	nS
T_{BEH}	C/BE#[3:0] (Byte Enable) Hold from CLK		2	–	nS
T_{ADS}	AD[31:0] (Address) Setup to CLK		7	–	nS
T_{ADH}	AD[31:0] (Address) Hold from CLK		2	–	nS
T_{DAS}	AD[31:0] (Data) Setup to CLK		7	–	nS
T_{DAH}	AD[31:0] (Data) Hold from CLK		2	–	nS
T_{DAD}	AD[31:0] (Data) Valid from CLK		2	11	nS
T_{TZH}	TRDY# High Z to High from CLK		2	11	nS
T_{THL}	TRDY# Active from CLK		2	11	nS
T_{TLH}	TRDY# Inactive from CLK		2	11	nS
T_{THZ}	TRDY# High before High Z		1	–	CLK
T_{DZL}	DEVSEL# Active from CLK		2	11	nS
T_{DLH}	DEVSEL# Inactive from CLK		2	11	nS
T_{DHZ}	DEVSEL# High before High Z		1	–	CLK
T_{ISC}	IRDY# Setup to CLK		7	–	nS
T_{IHC}	IRDY# Hold from CLK		2	–	nS

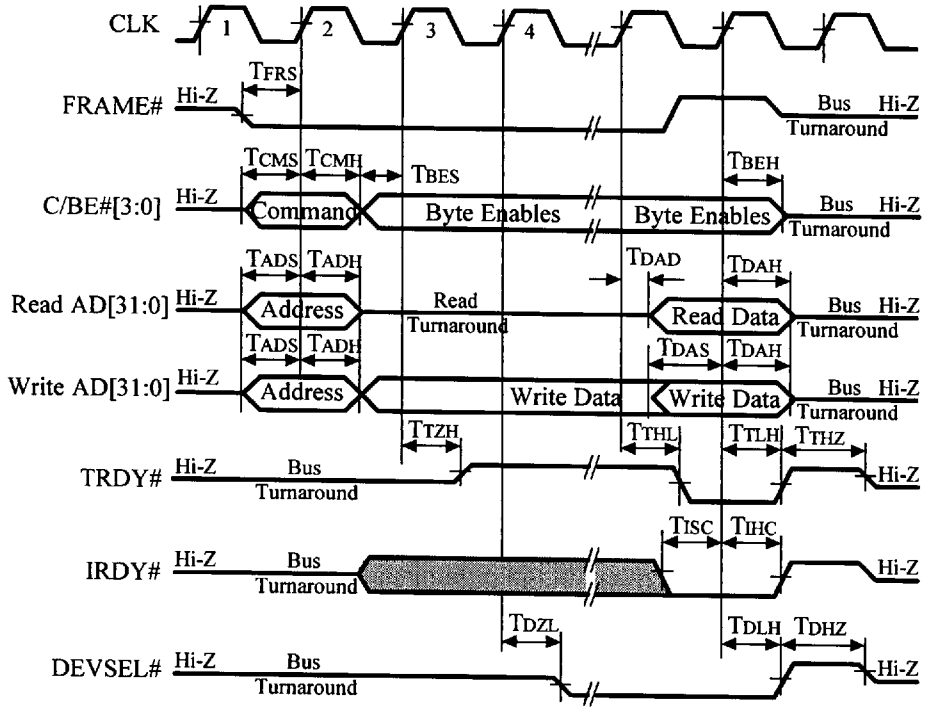


Figure 17-4: PCI Bus Frame Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

Table 17- 11: 65550 AC Timing Characteristics - PCI Bus Stop(33 MHz)

Symbol	Parameter	Notes	Min	Max	Units
T_{SZH}	STOP# High Z to High from CLK		2	11	nS
T_{SHL}	STOP# Active from CLK		2	11	nS
T_{SLH}	STOP# Inactive from CLK		2	11	nS
T_{SHZ}	STOP# High before High Z		1	—	CLK

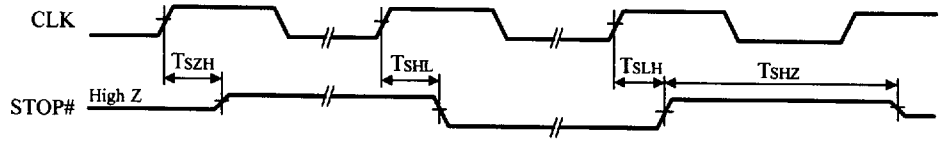


Figure 17-5: PCI Bus Stop Timing

Table 17- 12: 65550 AC Timing Characteristics PC BIOS ROM

Symbol	Parameter	Notes	Min	Max	Units
T_{ROE}	ROMOE# Active from CLK		–	40	nS

Note: PCI BIOS ROM timing is derived from the PCI bus clock. Timing sequences are fixed assuming the use of widely-available, low-cost, typical industry-standard EPROMs. Timing speci fications and performance of BIOS ROM memory access es are non-critical since PCI BIOS ROM data is always shadowed into high-speed system memory prior to execution of BIOS code.

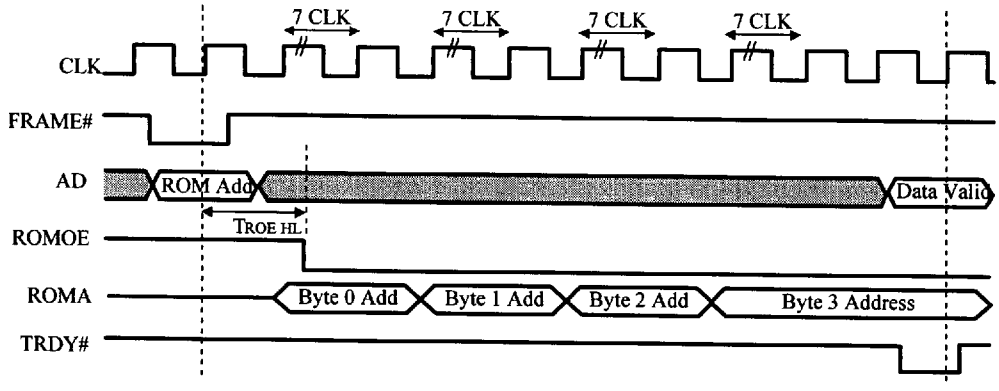


Figure 17-6: PCI BIOS ROM Timing

Table 17- 13: 65550 AC Timing Characteristics - DRAM Read / Write

Symbol	Parameter	Notes	Versions ES 2.0 and Earlier		Versions ES 2.1 and Later		Units
			Min	Max	Min	Max	
T_{RC}	Read/Write Cycle Time	Std DRAM	4Tm – 15	–	4Tm – 15	–	nS
		EDO DRAM	5Tm – 5	–	6Tm – 5	–	nS
T_{RAS}	RAS# Pulse Width	Std DRAM	2Tm – 5	–	2Tm – 5	–	nS
		EDO DRAM	3Tm – 5	–	4Tm – 5	–	nS
T_{RP}	RAS# Precharge	Std DRAM	2Tm – 5	–	2Tm – 5	–	nS
		EDO DRAM	2Tm – 5	–	2Tm – 5	–	nS
T_{CRP}	CAS# to RAS# Precharge	Std DRAM	2Tm – 15	–	2Tm – 15	–	nS
		EDO DRAM	2Tm – 15	–	2Tm – 15	–	nS
T_{CSH}	CAS# Hold from RAS#	Std DRAM	2Tm	–	2Tm	–	nS
		EDO DRAM	2Tm	–	3Tm-5	–	nS
T_{RCD}	RAS# to CAS# Delay	Std DRAM	1.5Tm – 10	1.5Tm	1.5Tm – 10	1.5Tm	nS
		EDO DRAM	1.5Tm – 10	–	2.5Tm – 5	–	nS
T_{RSH}	RAS# Hold from CAS#	Std DRAM	0.5Tm	–	0.5Tm	–	nS
		EDO DRAM	1.5Tm - 15	–	1.5Tm - 15	–	nS
T_{CP}	CAS# Precharge		–	0.5Tm	0.5Tm	–	nS
T_{CAS}	CAS# Pulse Width		–	0.5Tm	9.5	–	nS
T_{ASR}	Row Address Setup to RAS#		0.5Tm – 5	–	0.5Tm – 5	–	nS
T_{ASC}	Column Address Setup to CAS#	Std DRAM	0.5Tm	–	0.5Tm	–	nS
		EDO DRAM	0.5Tm – 5	–	0.5Tm – 5	–	nS
T_{RAH}	Row Address Hold from RAS#		Tm – 5	–	2Tm – 5	–	nS
T_{CAH}	Column Address Hold from CAS#		0.5Tm	–	0.5Tm	–	nS
T_{CAC}	Data Access Time from CAS#	Std DRAM	–	0.5Tm	–	0.5Tm	nS
		EDO DRAM	–	Tm-8	–	Tm-8	nS
T_{RAC}	Data Access Time from RAS#	Std DRAM	–	2Tm	–	2Tm	nS
		EDO DRAM	–	2.5Tm	–	4Tm-23	nS
T_{DS}	Write Data Setup to CAS#	Std DRAM	0.5Tm – 5		0.5Tm – 5		nS
		EDO DRAM	0.5Tm – 5		0.5Tm – 5		nS
T_{DH}	Write Data Hold from CAS#		0.5Tm		0.5Tm		nS
T_{COH}	Read data hold from CAS# fall	EDO DRAM	2		5		nS
T_{OFF}	Read data hold from CAS# rise	Std DRAM	0		0		nS
T_{PC}	CAS Cycle Time		Tm		Tm		nS
T_{WS}	WE# Setup to CAS#		Tm – 10		2Tm – 10		nS
T_{WH}	WE# Hold from CAS#		2Tm – 5		2Tm – 5		nS

Note: The 65550 does not perform mixed read and write (or read modify write) cycles during the sameCAS low interval
Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

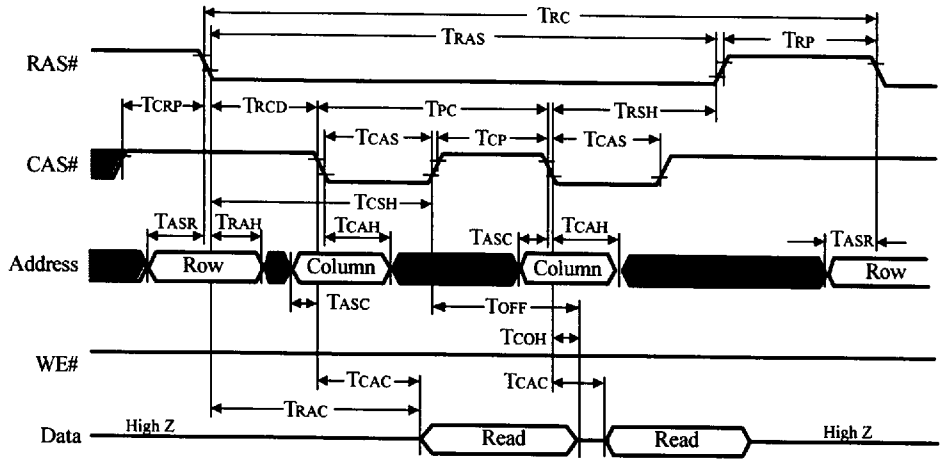


Figure 17-7: DRAM Page Mode Read Cycle Timing

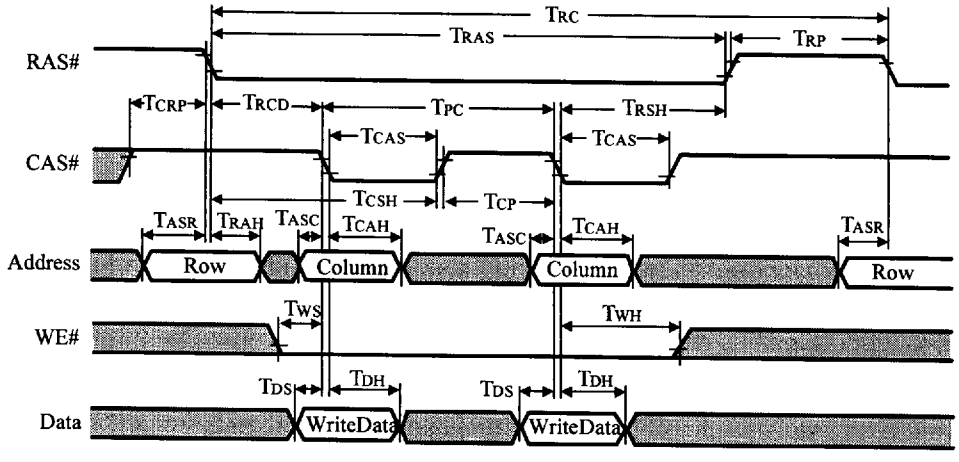


Figure 17-8: DRAM Page Mode Write Cycle Timing

Note: The above diagrams represent typical page mode cycles. The number of actual CAS cycles may vary.
Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

Table 17-14: 65550 AC Timing Characteristics - CBR Refresh

Symbol	Parameter	Notes	Min	Typical	Max	Units
T_{CHR}	RAS# to CAS# Delay		5Tm – 5	–	–	nS
T_{CSR}	CAS# to RAS# Delay	Normal Operation	Tm – 5	–	–	nS
		Standby Mode	2Tm – 5	–	–	nS
T_{RAS}	RAS# Pulse Width		5Tm – 5	–	–	nS

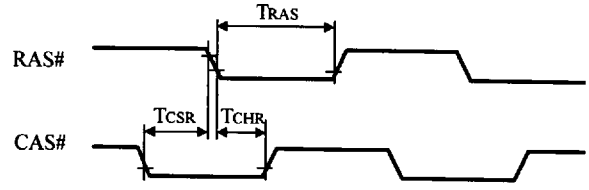


Figure 17-9: CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

Table 17-15: 65550 AC Timing Characteristics - Self Refresh

Symbol	Parameter	Notes	Min	Typical	Max	Units
T_{RASS}	RAS# Pulse Width for Self-Refresh		100	–	–	µS
T_{RP}	RAS# Precharge		4Tm – 3	–	–	nS
T_{RPS}	RAS# Precharge for Self-Refresh		10Tm	–	–	nS
T_{RPC}	RAS# to CAS# Delay		3Tm – 5	–	–	nS
T_{CSR}	CAS# to RAS# Delay	Normal Operation	Tm – 5	–	–	nS
		Standby Mode	2Tm – 5	–	–	nS
T_{CHS}	CAS# Hold Time		0	–	–	nS
T_{CPN}	CAS# Precharge		Tm – 5	–	–	nS

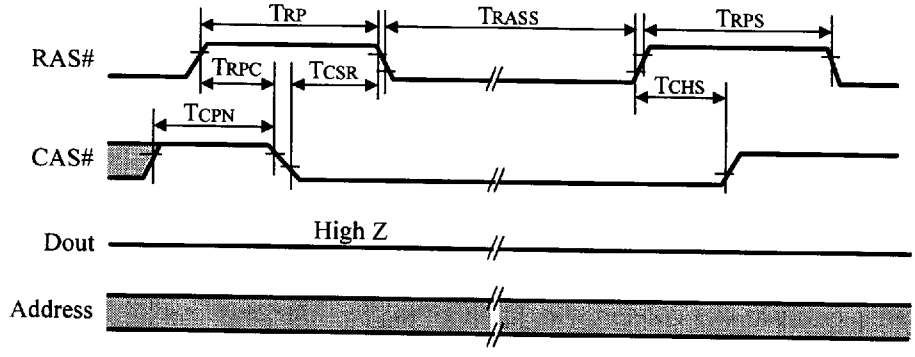


Figure 17-10: "Self Refresh DRAM" Refresh Cycle Timing

Table 17-16: 65550 AC Timing Characteristics - Video Data Port

Symbol	Parameter	Notes	Min	Max	Units
T_{VDS}	VP (Incoming Data) Setup	ZV-Port Mode	5*	–	nS
T_{VDH}	VP (Incoming Data) Hold		3*	–	nS
T_{HRS}	HREF (Incoming HS) Setup		5*	–	nS
T_{HRH}	HREF (Incoming HS) Hold		3*	–	nS
T_{VRS}	VREF (Incoming VS) Setup		5*	–	nS
T_{VRH}	VREF (Incoming VS) Hold		3*	–	nS

* Note: To be confirmed.

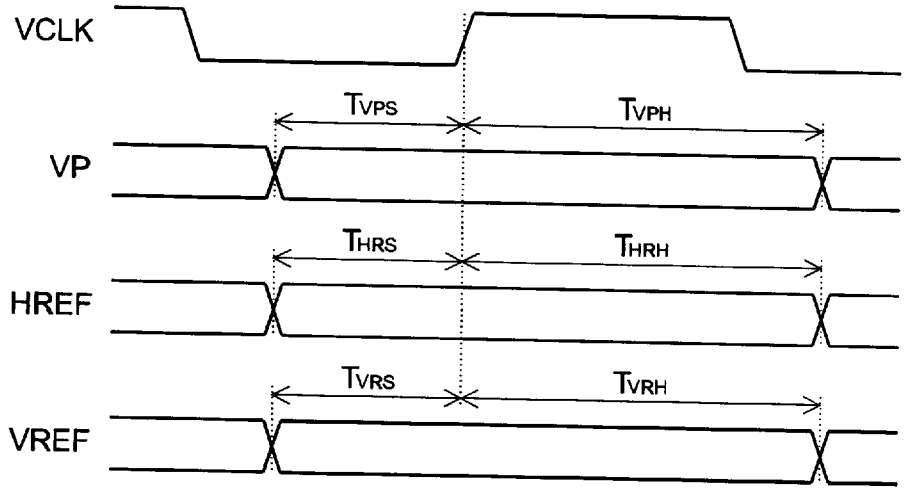


Figure 17-11: Video Data Port Timing

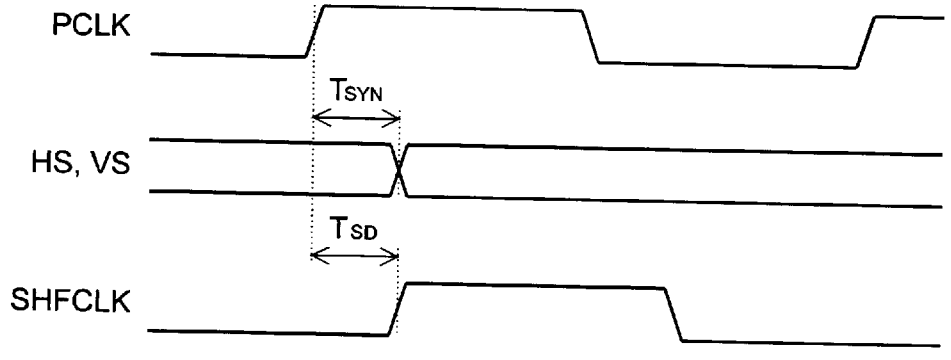


Figure 17-12: CRT Output Timing

Table 17- 17: 65550 AC Timing Characteristics - Panel Output Timing

Symbol	Parameter	Notes	Min	Max	Units
T_{SCCTR}	SHFCLK cycle time	Data latched on SHFCLK rise	15	–	nS
T_{SDR}	Panel data setup to SHFCLK rise		Tsc-5	–	nS
T_{HDR}	Panel data hold from SHFCLK rise		0	–	nS
T_{SCR}	Panel control setup to SHFCLK rise		Tsc-3	–	nS
T_{HCR}	Panel control hold from SHFCLK rise		-3	–	nS
T_{SCCTF}	SHFCLK cycle time	Data latched on SHFCLK fall	25	–	nS
T_{SDF}	Panel data setup to SHFCLK fall		0.5 Tsc-5	–	nS
T_{HDF}	Panel data hold from SHFCLK fall		0.5 Tsc	–	nS
T_{SCF}	Panel control setup to SHFCLK fall		0.5 Tsc-3	–	nS
T_{HCF}	Panel control hold from SHFCLK fall		0.5 Tsc-3	–	nS
T_{SCDC}	SHFCLK Duty Cycle (% high)	Color STN-DD or STN-SS	TBD	TBD	
	SHFCLK Duty Cycle (% high)	TFT or Mono STN	TBD	TBD	

Note: AC Timing is valid when either:
DVCC=5V, max output loading=50pF
DVCC=3.3V, max output loading=25pF.

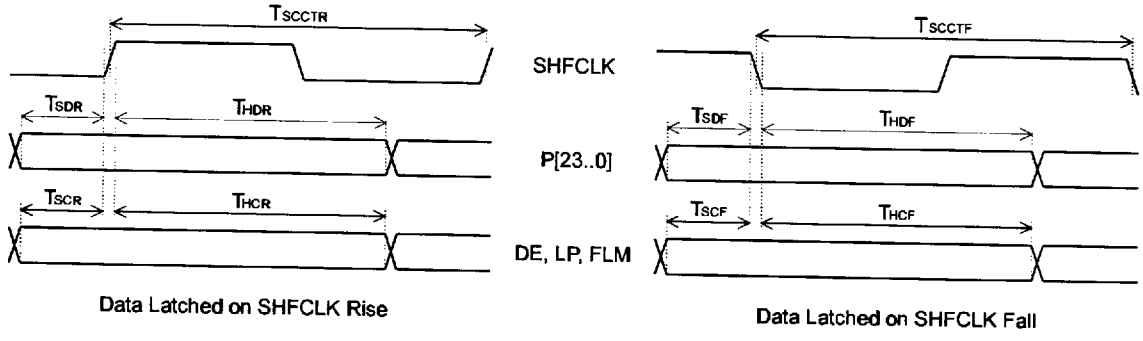


Figure 17-13: Panel Output Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

18.0 MECHANICAL SPECIFICATIONS

This sections provides the mechanical specifications for the Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), and Ball Grid Array (BGA).

18.1 Thin Quad Flat Pack (TQFP)

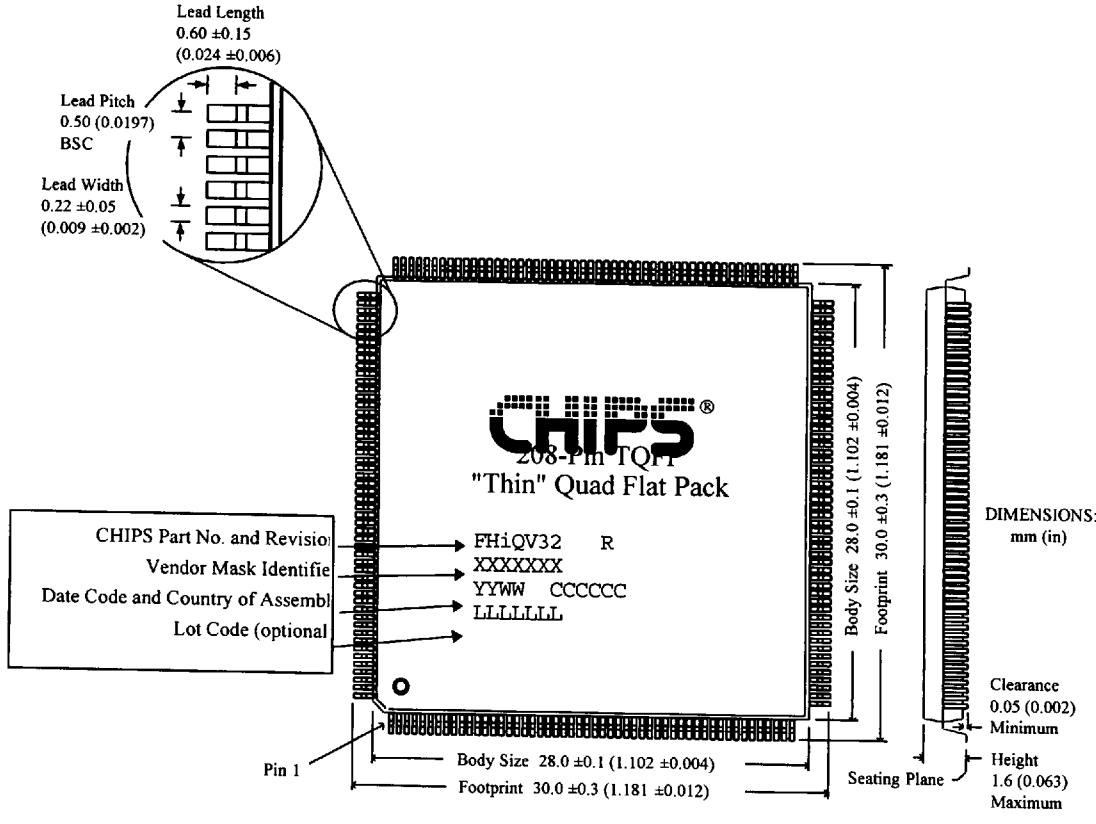


Figure 18-1: Thin Quad Flat Pack (TQFP)

18.2 Plastic Quad Flat Pack

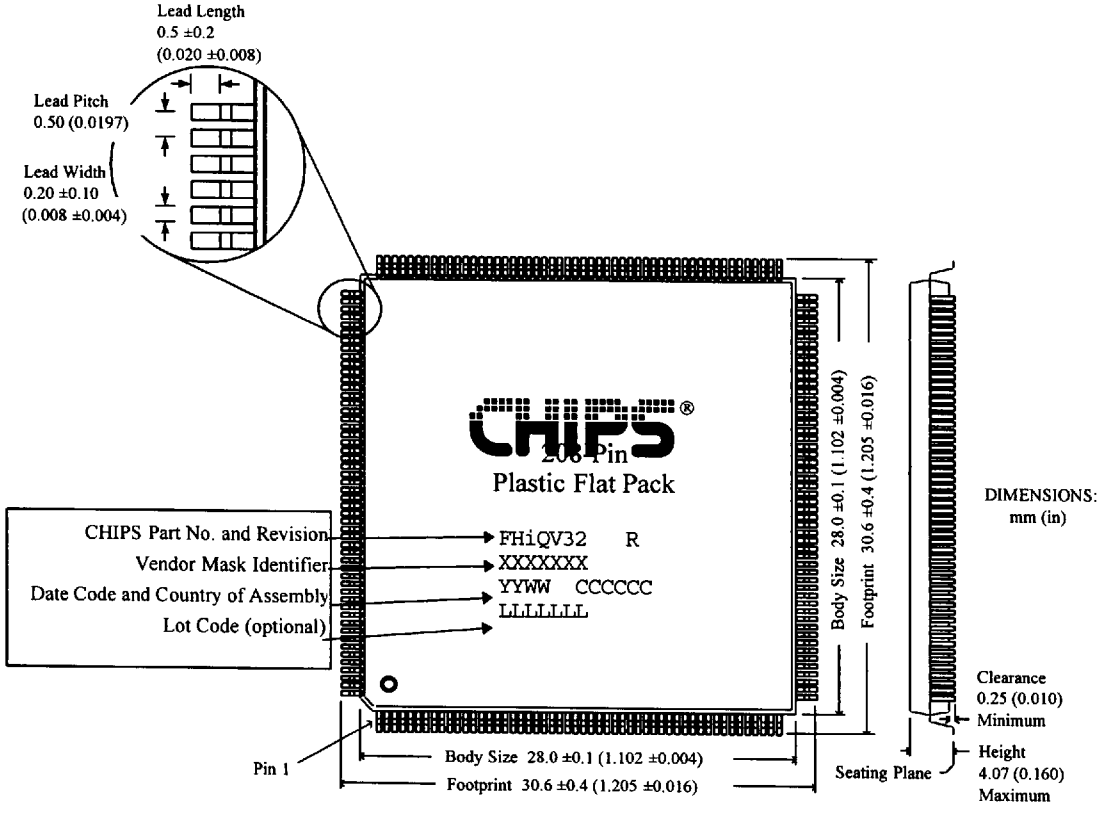
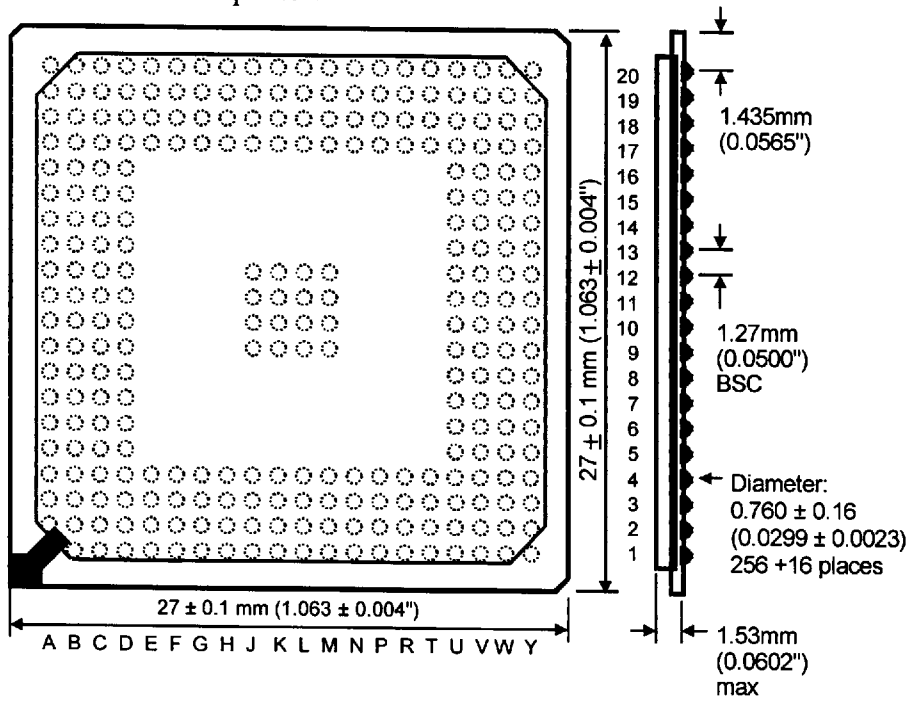


Figure 18-2: Plastic Quad Flat Pack

18.3 256+16-Contact Ball Grid Array

Top View



Bottom View

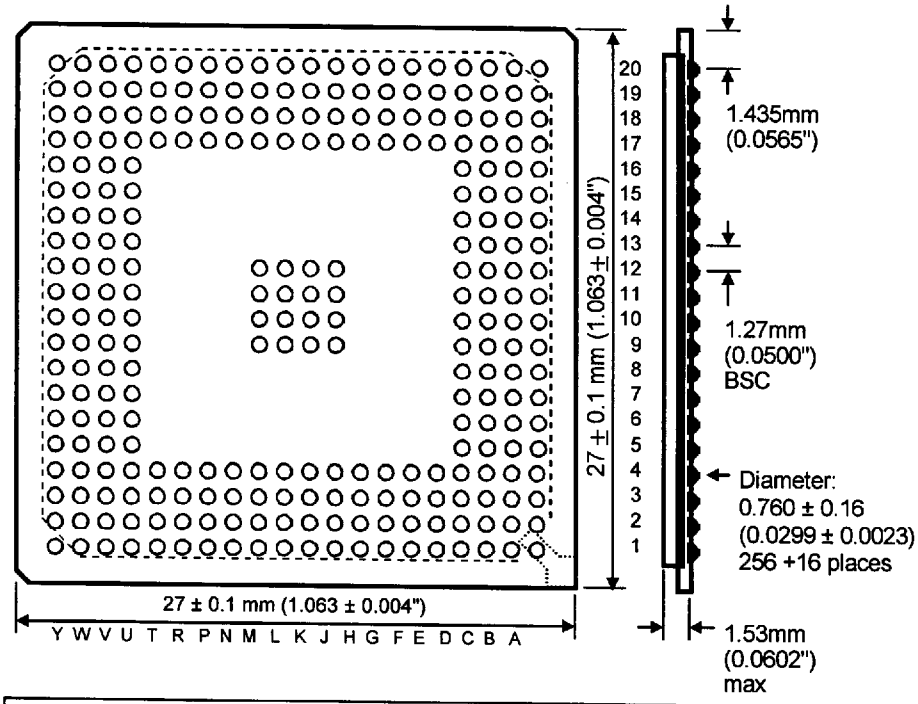


Figure 18-3: 256+16-Contact Ball Grid Array