

Dual-gate MOS-FETs**BF1100; BF1100R****FEATURES**

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source

and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1

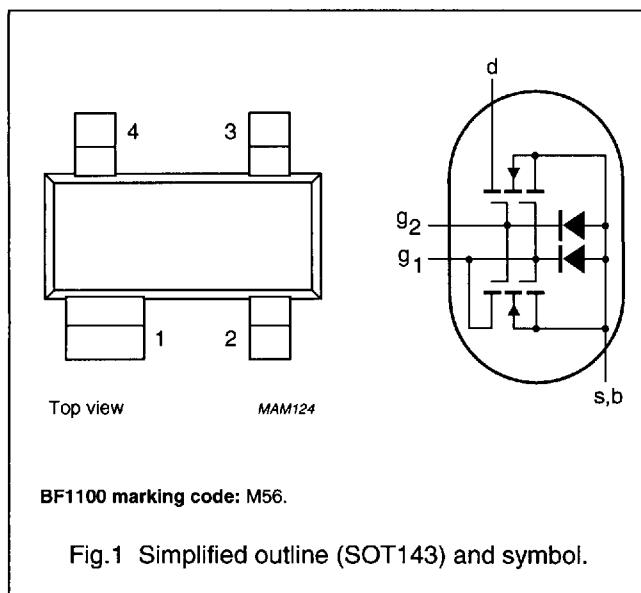


Fig.1 Simplified outline (SOT143) and symbol.

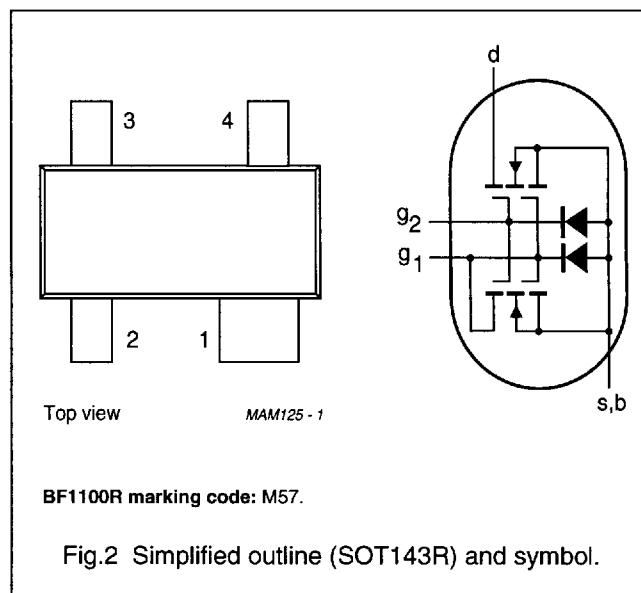


Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		—	—	14	V
I _D	drain current		—	—	30	mA
P _{tot}	total power dissipation		—	—	200	mW
T _j	operating junction temperature		—	—	150	°C
y _{fs}	forward transfer admittance		24	28	33	mS
C _{ig1-s}	input capacitance at gate 1		—	2.2	2.6	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	—	25	35	fF
F	noise figure	f = 800 MHz	—	2	—	dB

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	± 10	mA
I_{G2}	gate 2 current		–	± 10	mA
P_{tot}	total power dissipation BF1100 BF1100R	see Fig.3 up to $T_{amb} = 50^\circ\text{C}$; note 1 up to $T_{amb} = 40^\circ\text{C}$; note 1	–	200	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

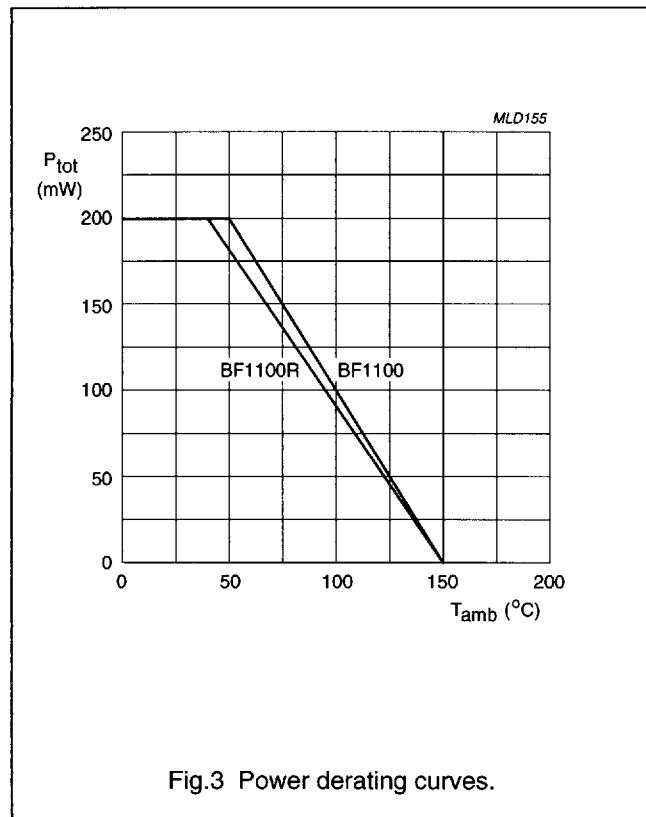


Fig.3 Power derating curves.

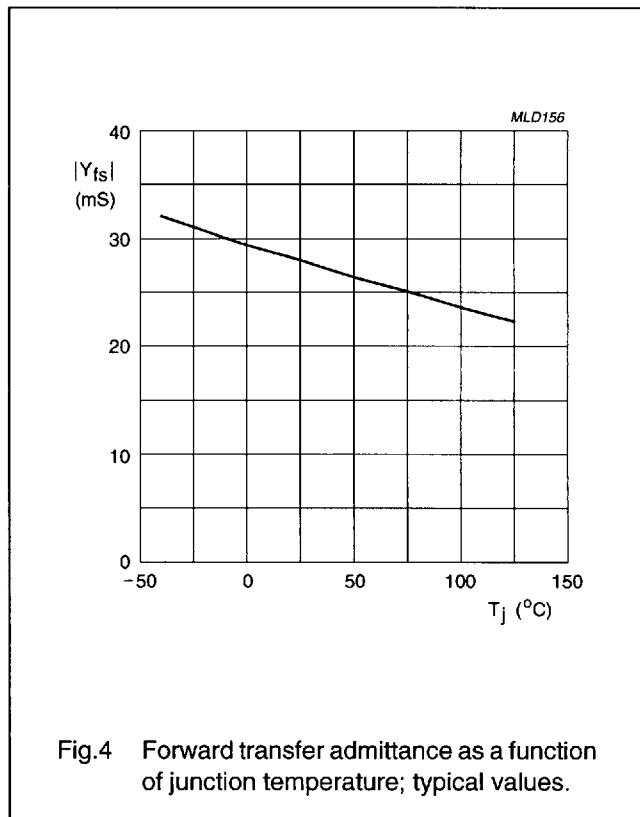


Fig.4 Forward transfer admittance as a function of junction temperature; typical values.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient BF1100 BF1100R	note 1	500 550	K/W K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point BF1100 BF1100R	note 2 $T_s = 92^\circ C$ $T_s = 78^\circ C$	290 360	K/W K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

 $T_j = 25^\circ C$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 1 \text{ mA}$	13.2	20	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 1 \text{ mA}$	13.2	20	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10 \text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10 \text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4 \text{ V}$; $V_{DS} = 9 \text{ V}$; $I_D = 20 \mu\text{A}$	0.3	1	V
		$V_{G2-S} = 4 \text{ V}$; $V_{DS} = 12 \text{ V}$; $I_D = 20 \mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 4 \text{ V}$; $V_{DS} = 9 \text{ V}$; $I_D = 20 \mu\text{A}$	0.3	1.2	V
		$V_{G1-S} = 4 \text{ V}$; $V_{DS} = 12 \text{ V}$; $I_D = 20 \mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4 \text{ V}$; $V_{DS} = 9 \text{ V}$; $R_{G1} = 180 \text{ k}\Omega$; note 1	8	13	mA
		$V_{G2-S} = 4 \text{ V}$; $V_{DS} = 12 \text{ V}$; $R_{G1} = 250 \text{ k}\Omega$; note 2	8	13	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 12 \text{ V}$	—	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 12 \text{ V}$	—	50	nA

Notes

1. R_{G1} connects gate 1 to $V_{GG} = 9 \text{ V}$; see Fig.27.
2. R_{G1} connects gate 1 to $V_{GG} = 12 \text{ V}$; see Fig.27.

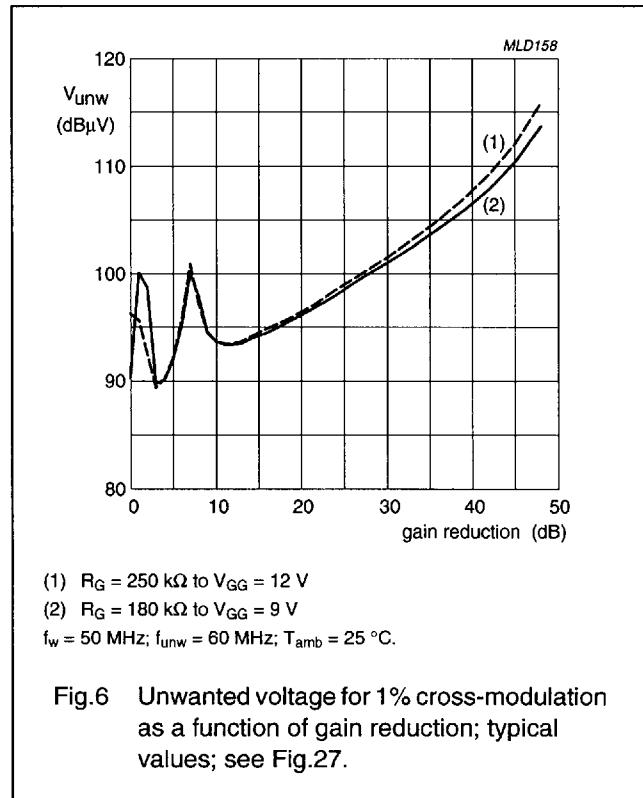
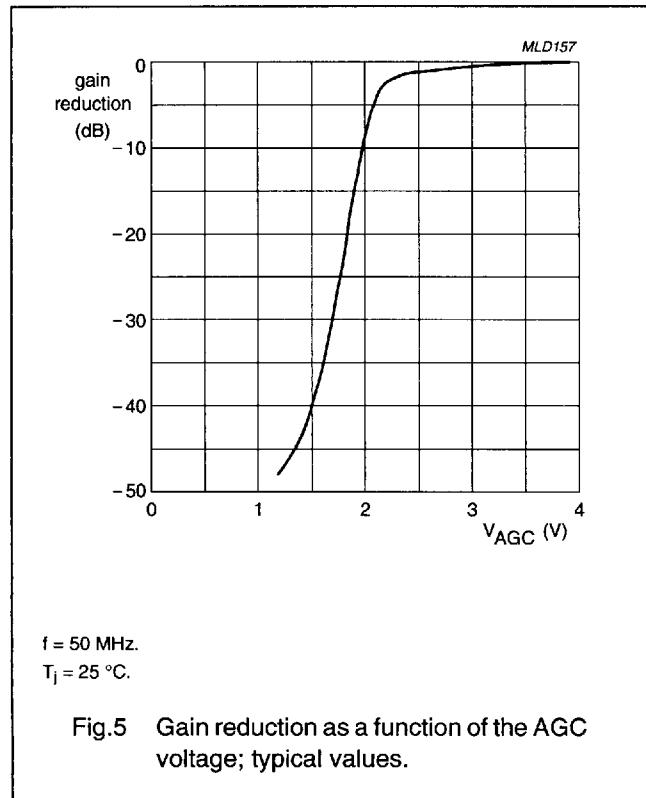
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DYNAMIC CHARACTERISTICS

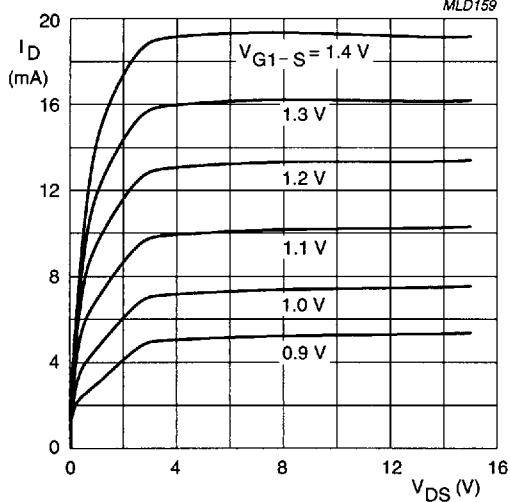
Common source; $T_{amb} = 25^\circ\text{C}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25^\circ\text{C}$ $V_{DS} = 9\text{ V}$ $V_{DS} = 12\text{ V}$	24 24	28 28	33 33	mS mS
C_{ig1-s}	input capacitance at gate 1	$f = 1\text{ MHz}$ $V_{DS} = 9\text{ V}$ $V_{DS} = 12\text{ V}$	— —	2.2 2.2	2.6 2.6	pF pF
C_{ig2-s}	input capacitance at gate 2	$f = 1\text{ MHz}$ $V_{DS} = 9\text{ V}$ $V_{DS} = 12\text{ V}$	— —	1.6 1.4	— —	pF pF
C_{os}	drain-source capacitance	$f = 1\text{ MHz}$ $V_{DS} = 9\text{ V}$ $V_{DS} = 12\text{ V}$	— —	1.4 1.1	1.8 1.5	pF pF
C_{rs}	reverse transfer capacitance	$f = 1\text{ MHz}$ $V_{DS} = 9\text{ V}$ $V_{DS} = 12\text{ V}$	— —	25 25	35 35	fF fF
F	noise figure	$f = 800\text{ MHz}$; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$ $V_{DS} = 9\text{ V}$ $V_{DS} = 12\text{ V}$	— —	2 2	2.8 2.8	dB dB



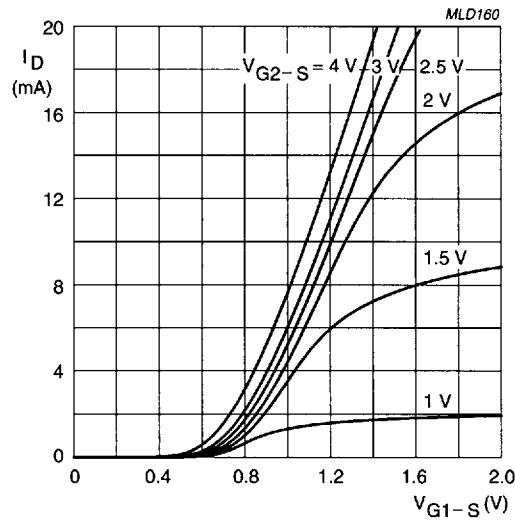
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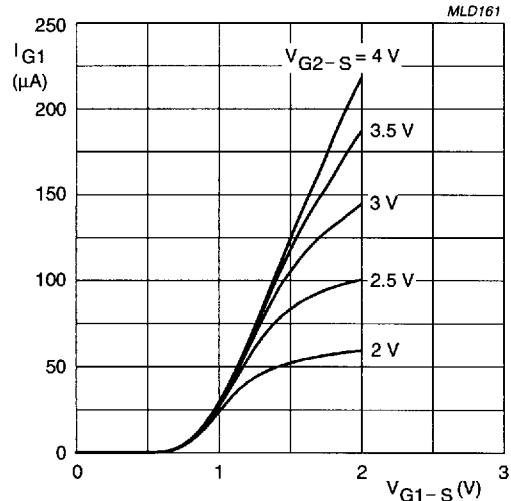
$V_{G2-S} = 4$ V.
 $T_j = 25$ °C.

Fig.7 Output characteristics; typical values.



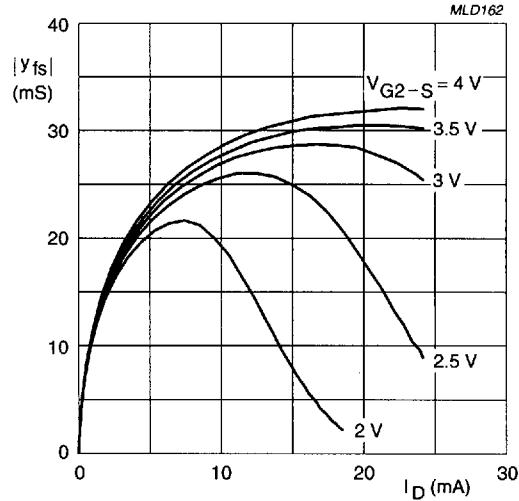
$V_{DS} = 9$ to 12 V.
 $T_j = 25$ °C.

Fig.8 Transfer characteristics; typical values.



$V_{DS} = 9$ to 12 V.
 $T_j = 25$ °C.

Fig.9 Gate 1 current as a function of gate 1 voltage; typical values.



$V_{DS} = 9$ to 12 V.
 $T_j = 25$ °C.

Fig.10 Forward transfer admittance as a function of drain current; typical values.

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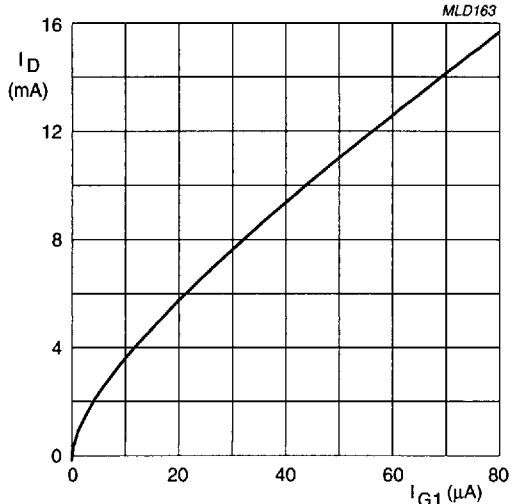
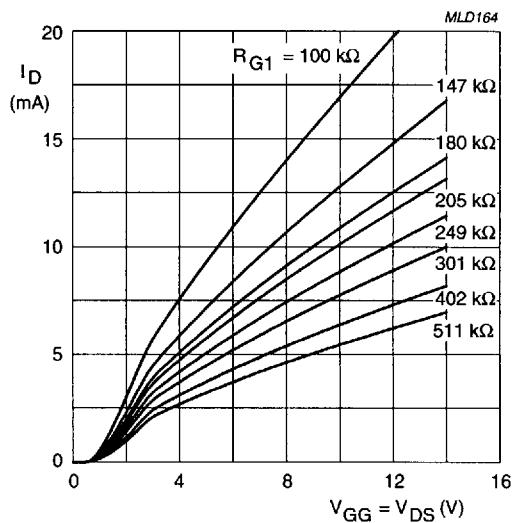
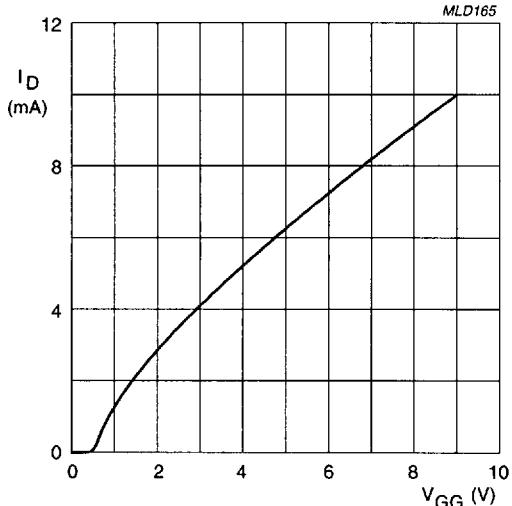
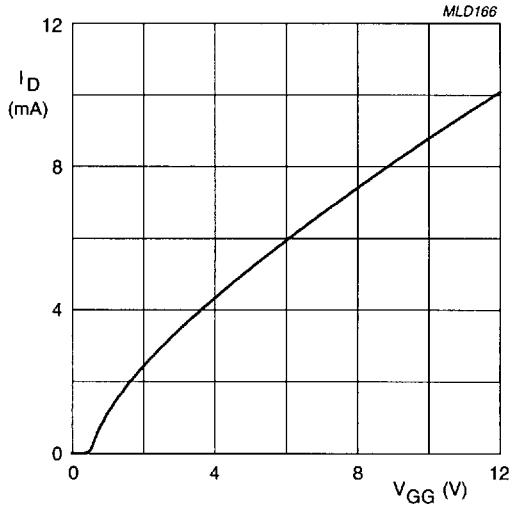
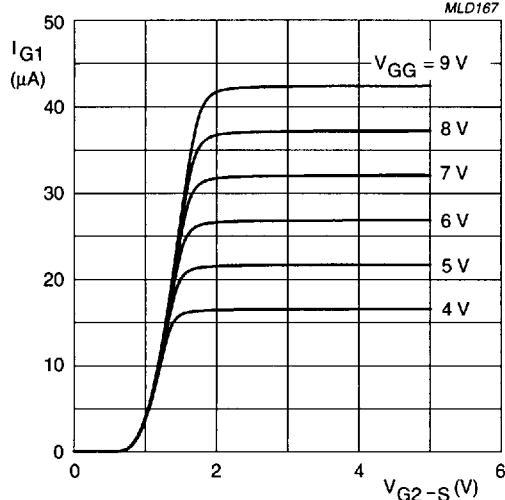
 $V_{DS} = 9$ to 12 V. $V_{G2-S} = 4$ V. $T_j = 25$ °C.

Fig.11 Drain current as a function of gate 1 current; typical values.

 $V_{G2-S} = 4$ V. R_{G1} connected to V_{GG} . $T_j = 25$ °C.Fig.12 Drain current as a function of gate 1 supply voltage ($= V_{GG}$) and drain supply voltage; typical values; see Fig.27. $V_{DS} = 9$ V; $V_{G2-S} = 4$ V. $R_{G1} = 180\text{ k}\Omega$ (connected to V_{GG}); $T_j = 25$ °C.Fig.13 Drain current as a function of gate 1 voltage ($= V_{GG}$); typical values; see Fig.27. $V_{DS} = 12$ V; $V_{G2-S} = 4$ V. $R_{G1} = 250\text{ k}\Omega$ (connected to V_{GG}); $T_j = 25$ °C.Fig.14 Drain current as a function of gate 1 voltage ($= V_{GG}$); typical values; see Fig.27.

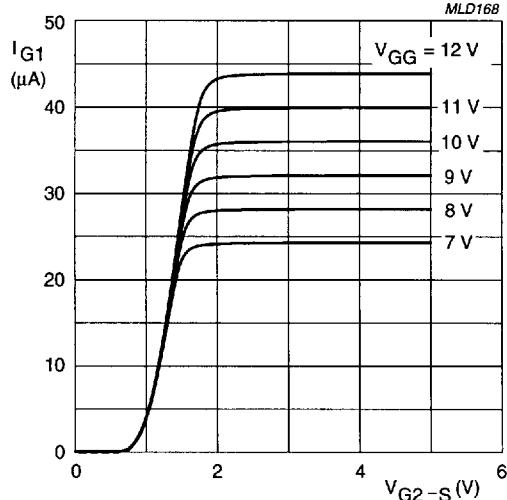
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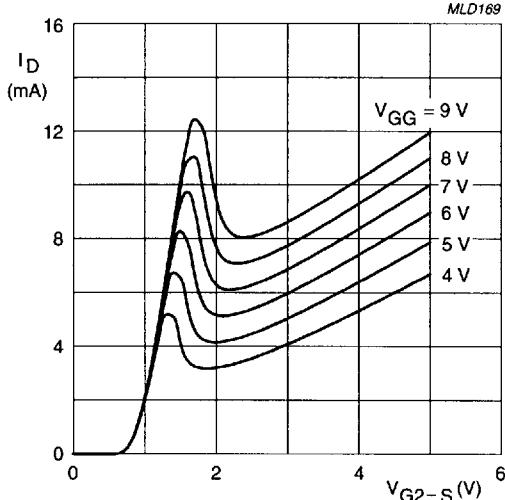
$V_{DS} = 9\text{ V}$.
 $R_{G1} = 180\text{ k}\Omega$ (connected to V_{GG}).
 $T_j = 25^\circ\text{C}$.

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.



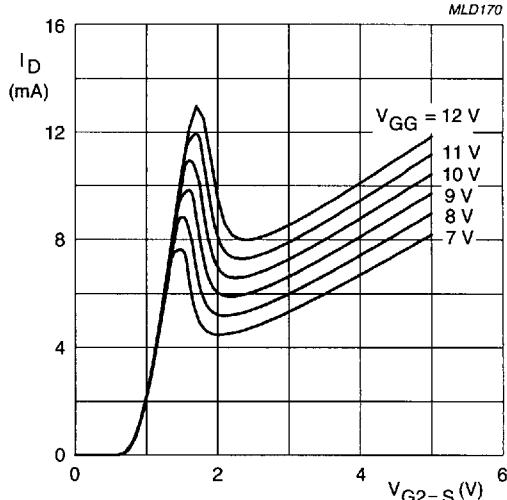
$V_{DS} = 12\text{ V}$.
 $R_{G1} = 250\text{ k}\Omega$ (connected to V_{GG}).
 $T_j = 25^\circ\text{C}$.

Fig.16 Gate 1 current as a function of gate 2 voltage; typical values.



$V_{DS} = 9\text{ V}$.
 $R_{G1} = 180\text{ k}\Omega$ (connected to V_{GG}).
 $T_j = 25^\circ\text{C}$.

Fig.17 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.

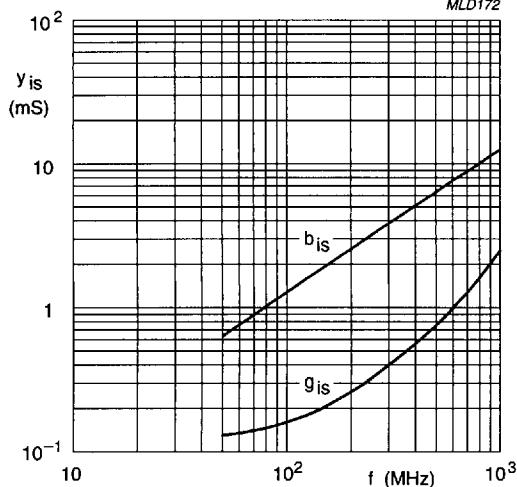


$V_{DS} = 12\text{ V}$.
 $R_{G1} = 250\text{ k}\Omega$ (connected to V_{GG}).
 $T_j = 25^\circ\text{C}$.

Fig.18 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.

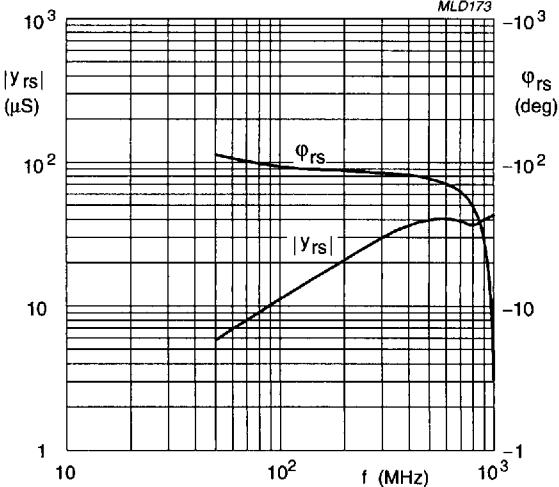
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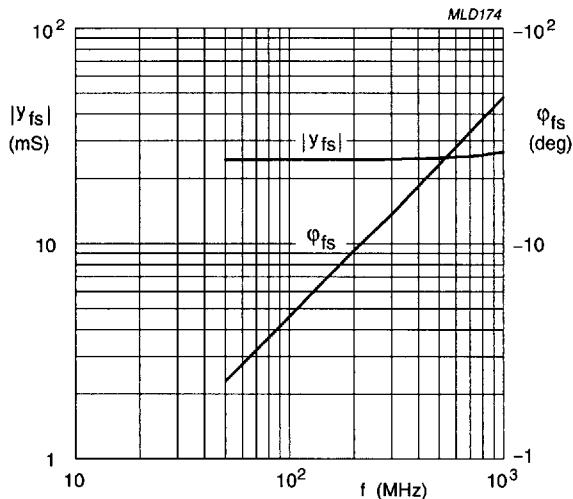
$V_{DS} = 9$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.19 Input admittance as a function of frequency; typical values.



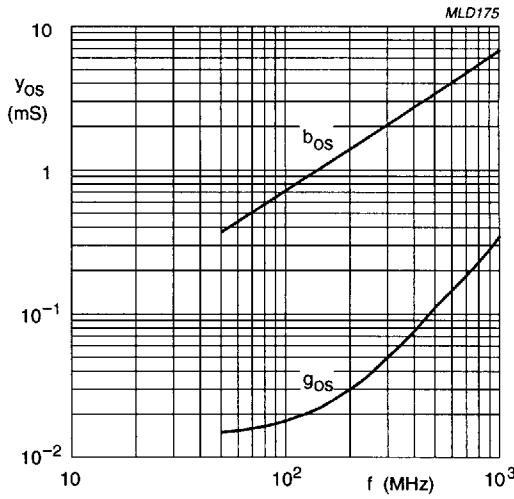
$V_{DS} = 9$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.20 Reverse transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 9$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.21 Forward transfer admittance and phase as a function of frequency; typical values.

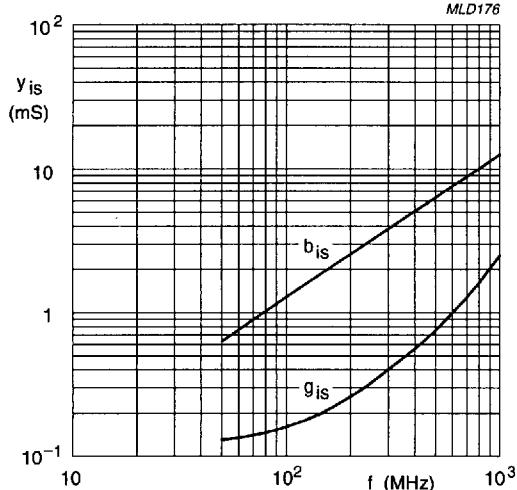


$V_{DS} = 9$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.22 Output admittance as a function of frequency; typical values.

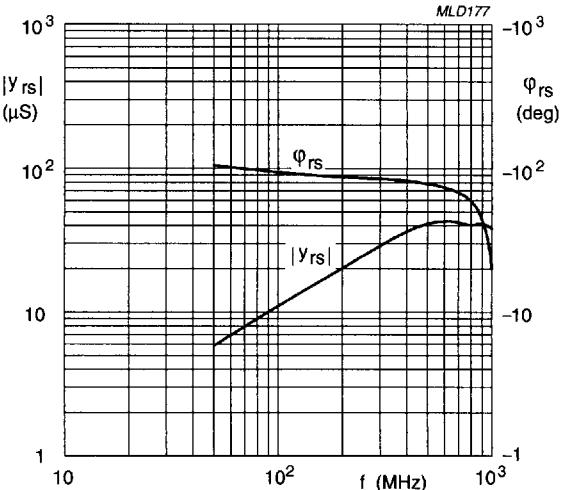
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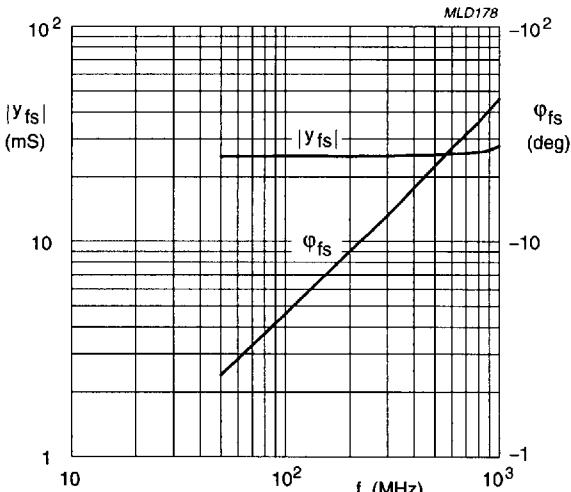
$V_{DS} = 12$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.23 Input admittance as a function of frequency; typical values.



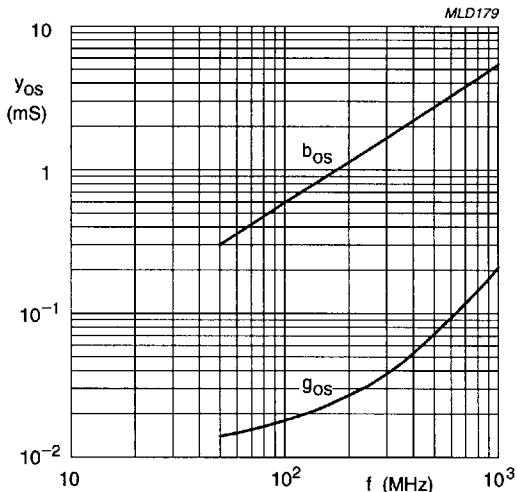
$V_{DS} = 12$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.24 Reverse transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 12$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.25 Forward transfer admittance and phase as a function of frequency; typical values.

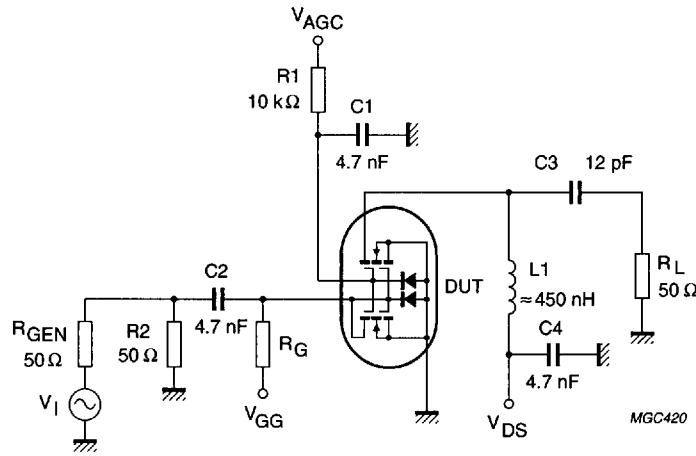


$V_{DS} = 12$ V; $V_{G2} = 4$ V.
 $I_D = 10$ mA; $T_{amb} = 25$ °C.

Fig.26 Output admittance as a function of frequency; typical values.

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For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ k Ω .

For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ k Ω .

Fig.27 Cross-modulation test set-up.

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Table 1 Scattering parameters: $V_{DS} = 9$ V; $V_{G2-S} = 4$ V; $I_D = 10$ mA

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	-3.6	2.528	174.4	0.001	63.7	1.000	-2.0
100	0.983	-7.4	2.531	169.8	0.001	80.7	1.000	-4.2
200	0.974	-14.7	2.490	159.5	0.002	81.0	0.996	-8.1
300	0.960	-21.8	2.446	149.8	0.002	80.3	0.994	-11.9
400	0.953	-28.7	2.412	139.8	0.003	76.3	0.992	-15.7
500	0.933	-35.4	2.341	130.1	0.003	76.5	0.987	-19.4
600	0.915	-42.0	2.283	120.4	0.004	79.0	0.984	-23.0
700	0.895	-47.9	2.205	111.6	0.003	81.5	0.981	-26.7
800	0.880	-53.5	2.146	102.9	0.003	90.8	0.978	-30.3
900	0.864	-59.6	2.087	93.4	0.003	106.6	0.974	-33.9
1000	0.839	-65.0	1.998	84.4	0.003	135.4	0.971	-37.6

Table 2 Noise data: $V_{DS} = 9$ V; $V_{G2-S} = 4$ V; $I_D = 10$ mA

f (MHz)	F _{min} (dB)	Γ _{opt}		r _n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

Table 3 Scattering parameters: $V_{DS} = 12$ V; $V_{G2-S} = 4$ V; $I_D = 10$ mA

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	-3.7	2.478	174.7	0.001	72.2	1.000	-1.6
100	0.984	-7.4	2.480	170.3	0.001	80.9	1.000	-3.5
200	0.974	-14.6	2.440	160.6	0.002	82.7	0.997	-6.6
300	0.960	-21.8	2.400	151.4	0.002	79.9	0.996	-9.7
400	0.953	-28.7	2.371	141.9	0.003	77.7	0.994	-12.8
500	0.933	-35.3	2.306	132.7	0.003	77.1	0.991	-15.8
600	0.915	-41.9	2.255	123.6	0.004	77.1	0.989	-18.7
700	0.894	-47.8	2.183	115.3	0.004	79.3	0.986	-21.7
800	0.879	-53.5	2.131	107.2	0.003	83.9	0.984	-24.6
900	0.863	-59.5	2.080	98.2	0.003	95.1	0.982	-27.5
1000	0.838	-65.0	1.999	89.7	0.003	115.8	0.980	-30.4

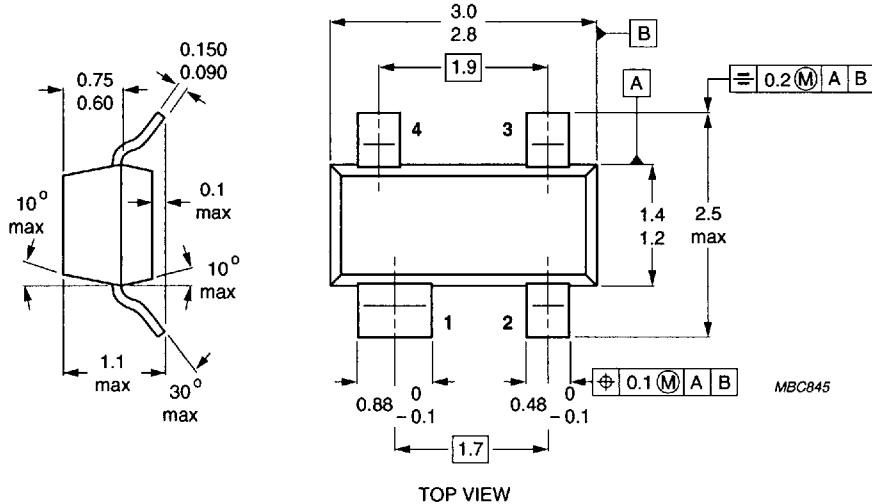
Table 4 Noise data: $V_{DS} = 12$ V; $V_{G2-S} = 4$ V; $I_D = 10$ mA

f (MHz)	F _{min} (dB)	Γ _{opt}		r _n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

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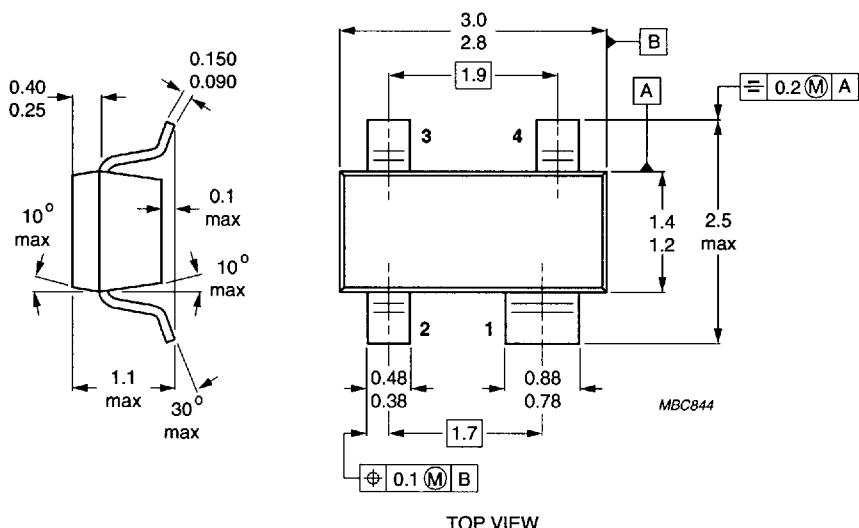
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PACKAGE OUTLINES



Dimensions in mm.

Fig.28 SOT143.



Dimensions in mm.

Fig.29 SOT143R.