

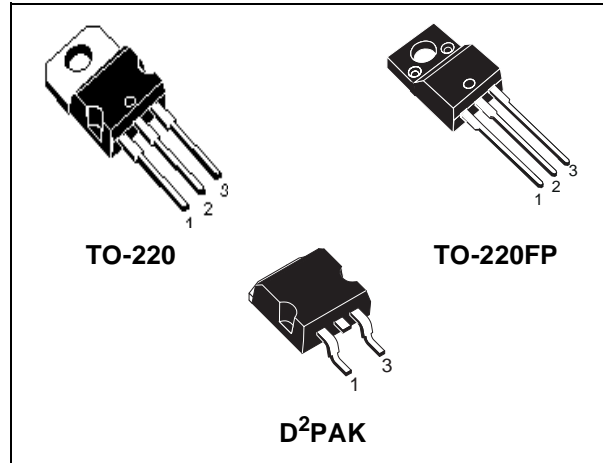


# STP11NK40Z - STP11NK40ZFP STB11NK40Z

N-CHANNEL 400V - 0.49Ω - 9A TO-220/TO-220FP/D<sup>2</sup>PAK  
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP11NK40Z	400 V	< 0.55 Ω	9 A	110 W
STP11NK40ZFP	400 V	< 0.55 Ω	9 A	30 W
STB11NK40Z	400 V	< 0.55 Ω	9 A	110 W

- TYPICAL R<sub>DS(on)</sub> = 0.49 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



## DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

## INTERNAL SCHEMATIC DIAGRAM



## ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP11NK40Z	P11NK40Z	TO-220	TUBE
STP11NK40ZFP	P11NK40ZFP	TO-220FP	TUBE
STB11NK40ZT4	B11NK40Z	D <sup>2</sup> PAK	TAPE & REEL

## STP11NK40Z - STP11NK40ZFP - STB11NK40Z

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP11NK40Z STB11NK40Z	STP11NK40ZFP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	400		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	400		V
V <sub>GS</sub>	Gate- source Voltage	± 30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	9	9(*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	5.67	5.67(*)	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	36	36(*)	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	110	30	W
	Derating Factor	0.88	0.24	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3500		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V <sub>iso</sub>	Insulation Withstand Voltage (DC)	--	2500	V
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		°C °C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 9A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(\*) Limited only by maximum temperature allowed

### THERMAL DATA

		TO-220 D <sup>2</sup> PAK	TO-220FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.14	4.2	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	9	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	190	mJ

### GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	I <sub>gs</sub> = ± 1mA (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## STP11NK40Z - STP11NK40ZFP - STB11NK40Z

### ELECTRICAL CHARACTERISTICS (TCASE = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	400			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125 \text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100 \mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$		0.49	0.55	$\Omega$

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 4.5 \text{ A}$		5.8		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		930 140 30		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V to } 400 \text{ V}$		78		pF

### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 200 \text{ V}, I_D = 4.5 \text{ A}$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		20 20		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 320 \text{ V}, I_D = 9 \text{ A},$ $V_{GS} = 10 \text{ V}$		32 6 18.5	45	nC nC nC

### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 200 \text{ V}, I_D = 4.5 \text{ A}$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		40 18		ns ns
$t_r(V_{off})$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 320 \text{ V}, I_D = 9 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (Inductive Load see, Figure 5)		15 17 30		ns ns ns

### SOURCE DRAIN DIODE

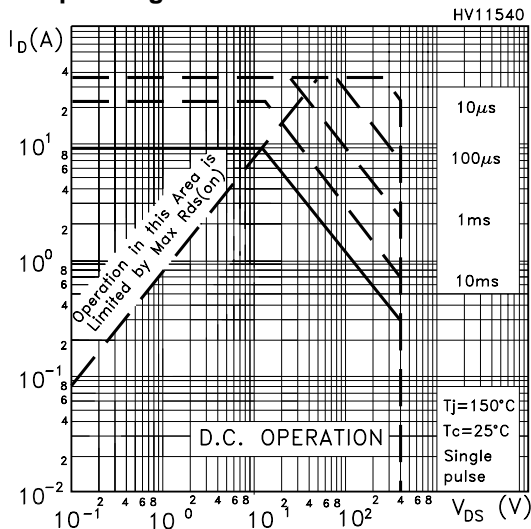
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				9 36	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 9 \text{ A}, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 9 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 45 \text{ V}, T_J = 150 \text{ °C}$ (see test circuit, Figure 5)		225 1.6 14		ns $\mu\text{C}$ A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

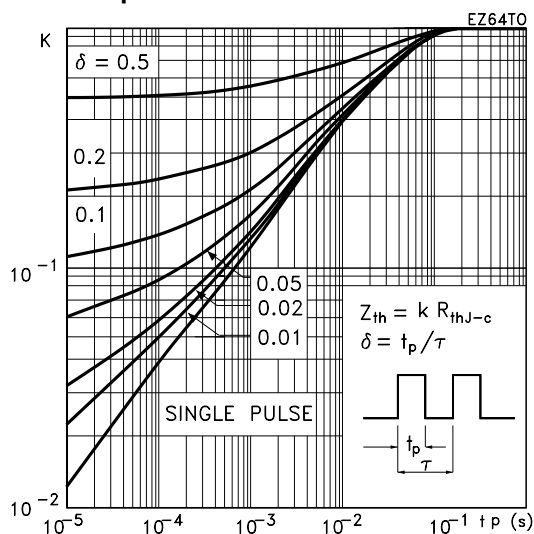
2. Pulse width limited by safe operating area.

3.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

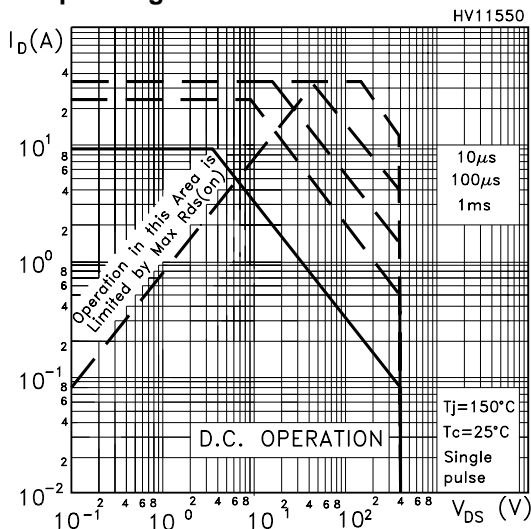
Safe Operating Area For TO-220/D2PAK



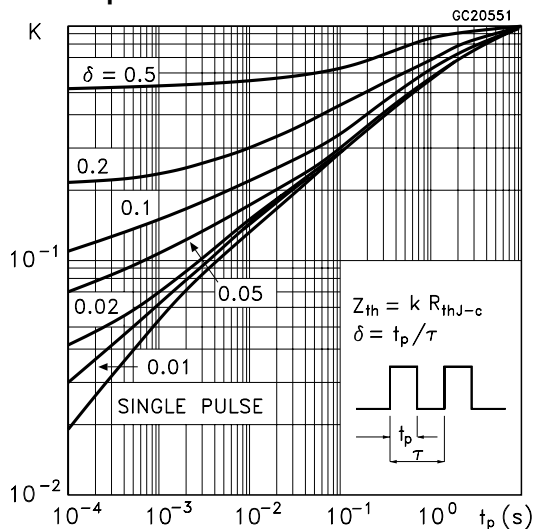
Thermal Impedance For TO-220/D2PAK



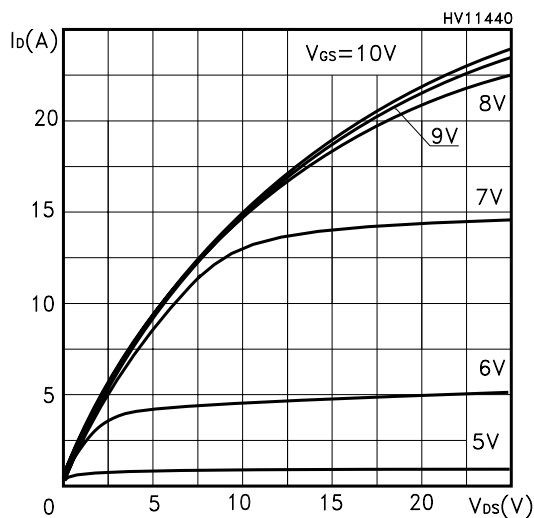
Safe Operating Area For TO-220FP



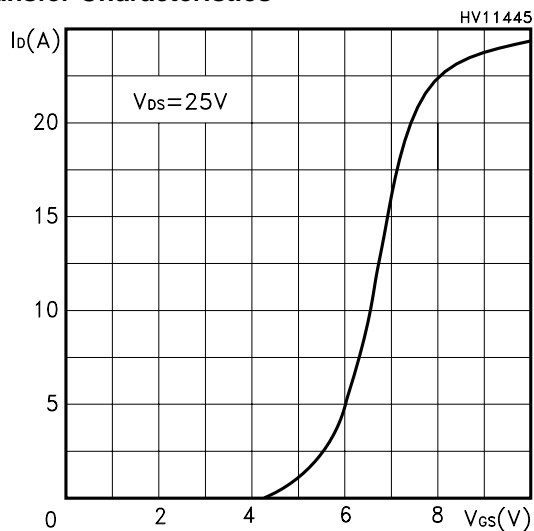
Thermal Impedance For TO-220FP



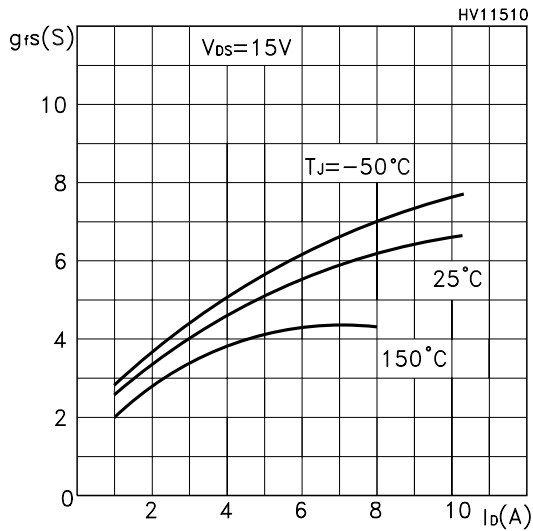
Output Characteristics



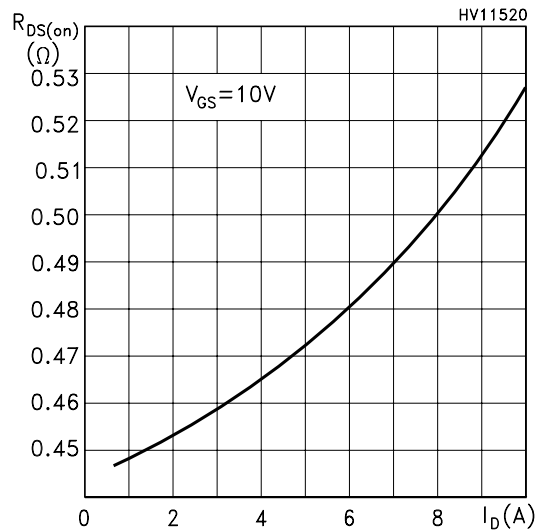
Transfer Characteristics



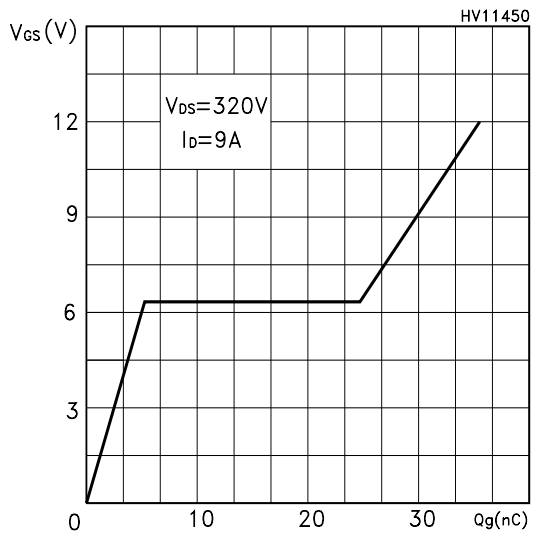
**Transconductance**



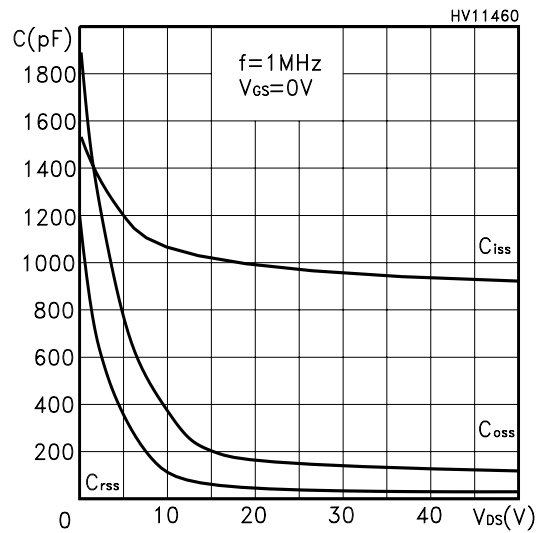
**Static Drain-source On Resistance**



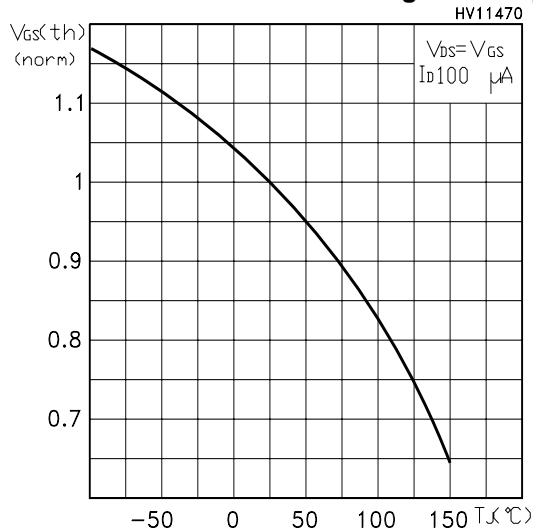
**Gate Charge vs Gate-source Voltage**



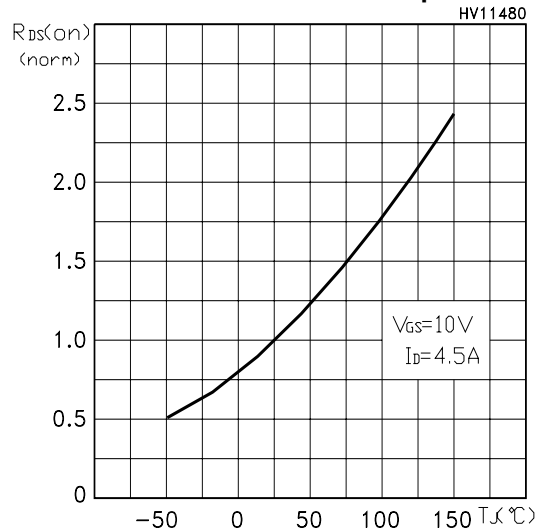
**Capacitance Variations**



**Normalized Gate Threshold Voltage vs Temp.**

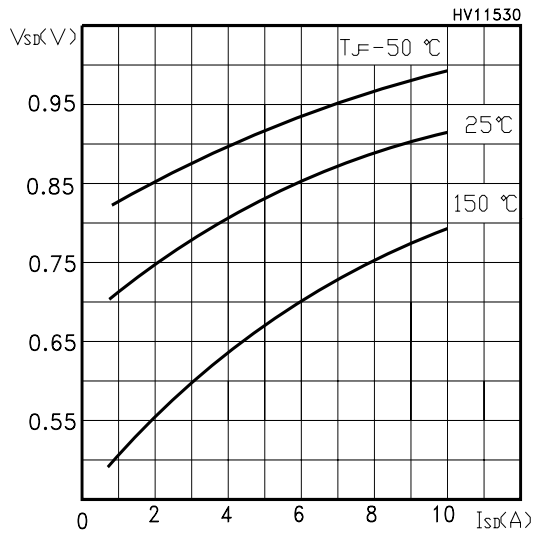


**Normalized On Resistance vs Temperature**

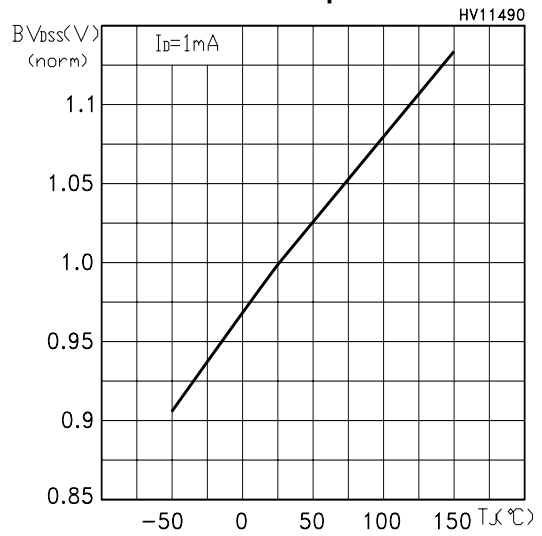


**STP11NK40Z - STP11NK40ZFP - STB11NK40Z**

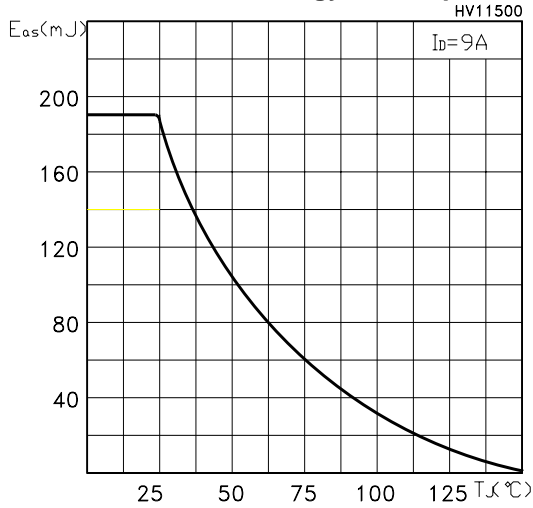
**Source-drain Diode Forward Characteristics**



**Normalized BVDSS vs Temperature**



**Maximum Avalanche Energy vs Temperature**



**Fig. 1: Unclamped Inductive Load Test Circuit**



**Fig. 2: Unclamped Inductive Waveform**



**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**



**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



**TO-220 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151

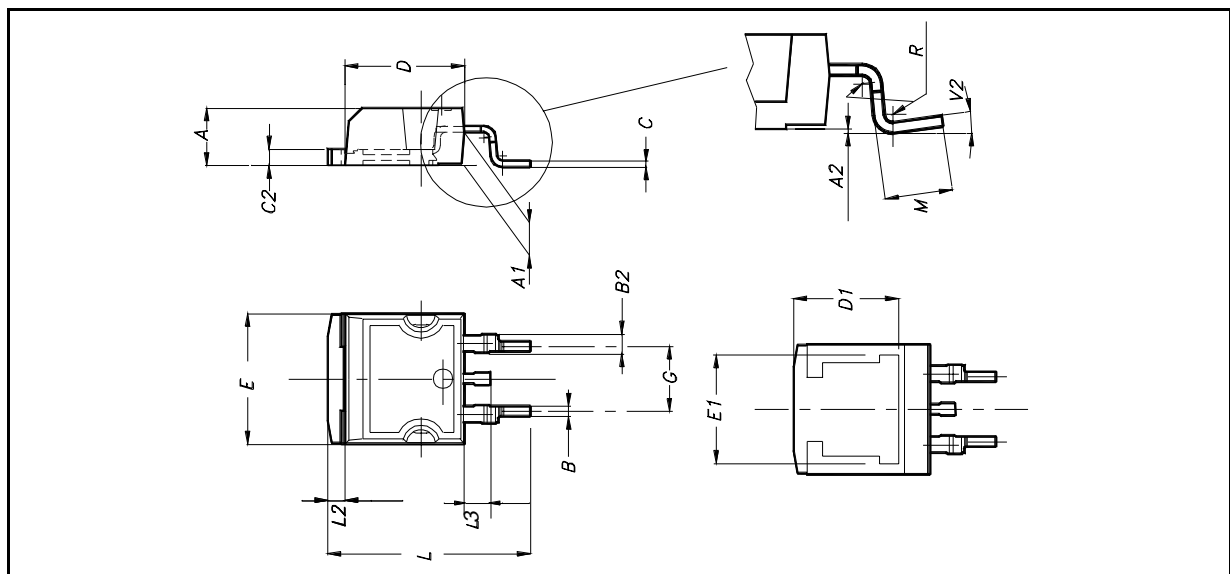




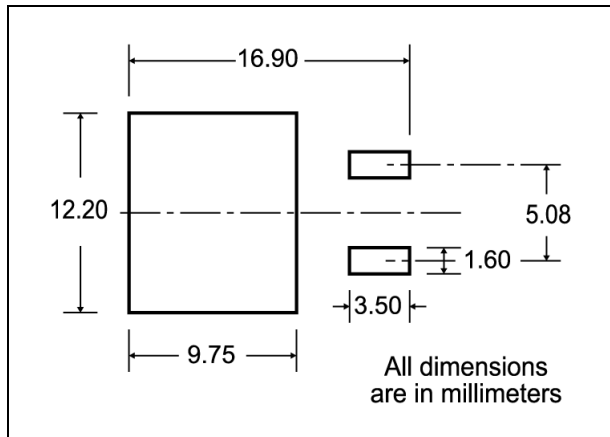


**D<sup>2</sup>PAK MECHANICAL DATA**

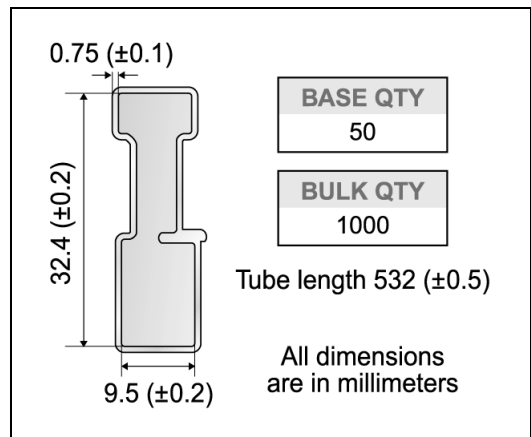
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



**D<sup>2</sup>PAK FOOTPRINT**



**TUBE SHIPMENT (no suffix)\***



**TAPE AND REEL SHIPMENT (suffix "T4")\***

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

<b>BASE QTY</b>	1000
<b>BULK QTY</b>	1000

10 pitches cumulative tolerance on tape +/− 0.2 mm

Center line of cavity

Bending radius

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