

SN74ALVCH16525

18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES059D – NOVEMBER 1995 – REVISED SEPTEMBER 1999

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}) and clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select (\overline{SEL}) input.

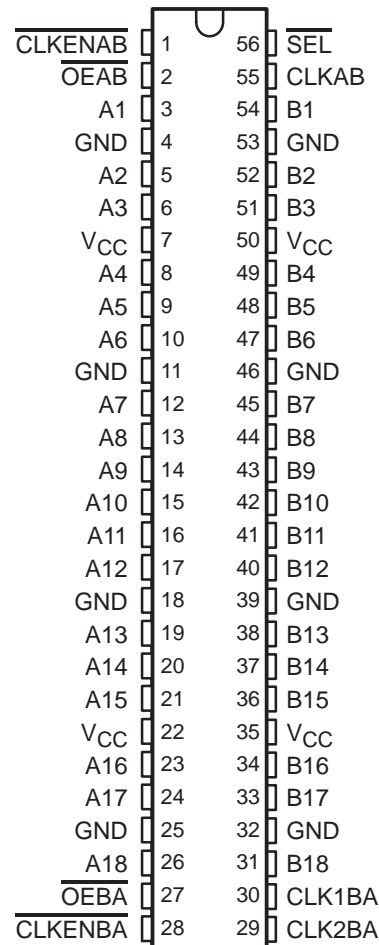
Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate \overline{CLKEN} inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16525 is characterized for operation from -40°C to 85°C .

**DGG OR DL PACKAGE
(TOP VIEW)**



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Function Tables

A-TO-B STORAGE
($\overline{OEAB} = L$)

INPUTS			OUTPUT B
$\overline{CLKENAB}$	CLKAB	A	
H	X	X	B_0^\dagger
L	↑	L	L
L	↑	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE
($\overline{OEBA} = L$)

INPUTS					OUTPUT A
$\overline{CLKENBA}$	CLK2BA	CLK1BA	\overline{SEL}	B	
H	X	X	X	X	A_0^\dagger
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L^\ddagger
L	↑	↑	L	H	H^\ddagger

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when \overline{SEL} is low.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT	
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V	
	I _{OH} = -4 mA	1.65 V	1.2				
	I _{OH} = -6 mA	2.3 V	2				
	I _{OH} = -12 mA	2.3 V	1.7				
		2.7 V	2.2				
		3 V	2.4				
I _{OH} = -24 mA	3 V	2					
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.2			V	
	I _{OL} = 4 mA	1.65 V	0.45				
	I _{OL} = 6 mA	2.3 V	0.4				
	I _{OL} = 12 mA	2.3 V	0.7				
		2.7 V	0.4				
	I _{OL} = 24 mA	3 V	0.55				
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA	
I _I (hold)	V _I = 0.58 V	1.65 V	25			μA	
	V _I = 1.07 V	1.65 V	-25				
	V _I = 0.7 V	2.3 V	45				
	V _I = 1.7 V	2.3 V	-45				
	V _I = 0.8 V	3 V	75				
	V _I = 2 V	3 V	-75				
	V _I = 0 to 3.6 V‡	3.6 V	±500				
I _{OZ} §	V _O = V _{CC} or GND	3.6 V	±10			μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			μA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	7			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	†		120		125		150		MHz
t _w	Pulse duration, CLK high or low	†		3.2		3.2		3		ns
t _{su}	Setup time	A data before CLKAB↑		†		1.3		1.3		ns
		B data before CLK2BA↑		†		2.1		1.8		
		B data before CLK1BA↑		†		1.3		1.2		
		SEL before CLK2BA↑		†		3.3		3.3		
		CLKENAB before CLKAB↑		†		2.1		1.9		
		CLKENBA before CLK1BA↑		†		2.7		2.5		
		CLKENBA before CLK2BA↑		†		2.7		2.5		
t _h	Hold time	A data after CLKAB↑		†		0.7		0.4		ns
		B data after CLK2BA↑		†		0.4		0		
		B data after CLK1BA↑		†		0.8		0.4		
		SEL after CLK2BA↑		†		0		0		
		CLKENAB after CLKAB↑		†		0.1		0.3		
		CLKENBA after CLK1BA↑		†		0		0		
		CLKENBA after CLK2BA↑		†		0		0		

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		120		125		150		MHz
t _{pd}	CLKAB or CLK2BA	A or B		†	1	4.5	4.4		1	4.2	ns
t _{en}	OEAB or OEBA	A or B		†	1	6.1	6.1		1	5.1	ns
t _{dis}	OEAB or OEBA	A or B		†	1	6.3	5.4		1	4.9	ns

† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

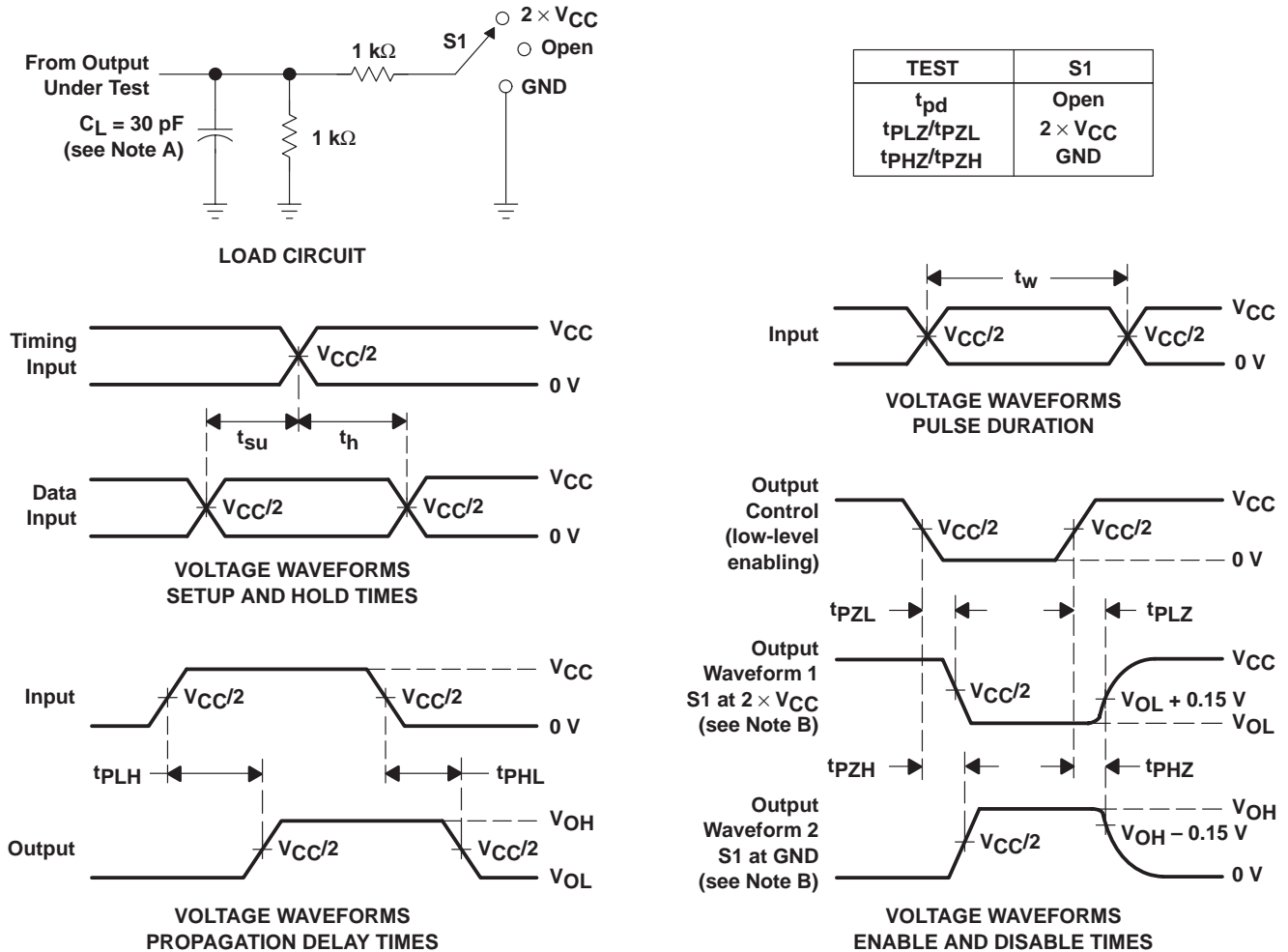
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	Outputs enabled	†	160	160	pF
		Outputs disabled	†	160	160	

† This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

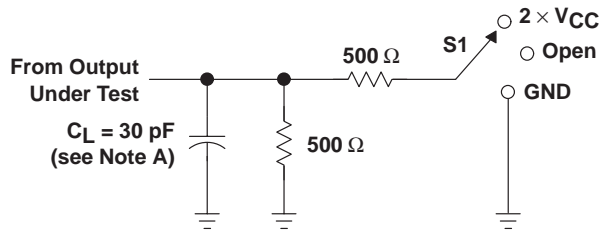
Figure 1. Load Circuit and Voltage Waveforms

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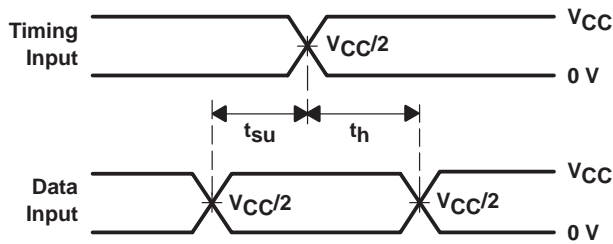
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$

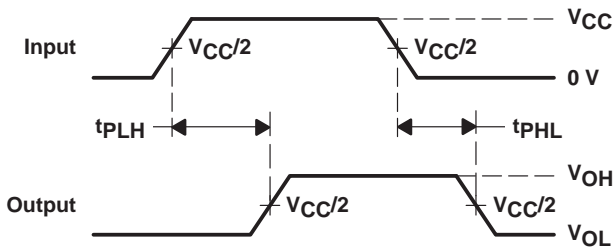


LOAD CIRCUIT

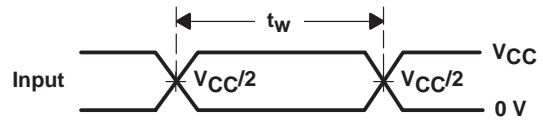
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



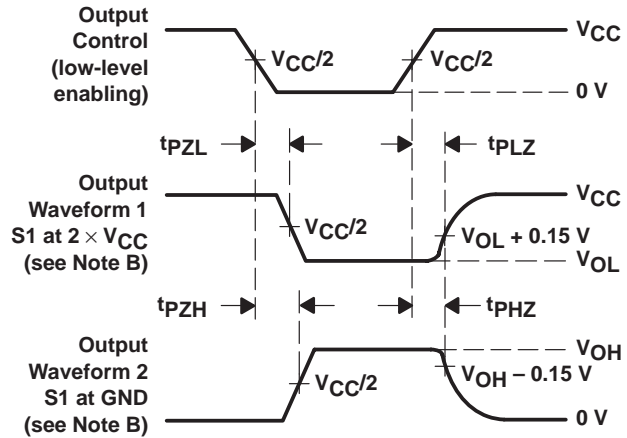
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



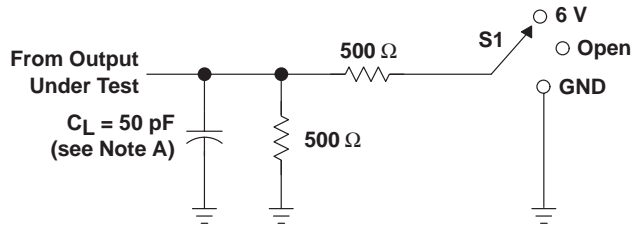
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
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Figure 2. Load Circuit and Voltage Waveforms

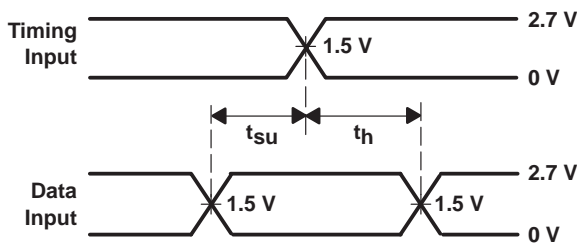
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

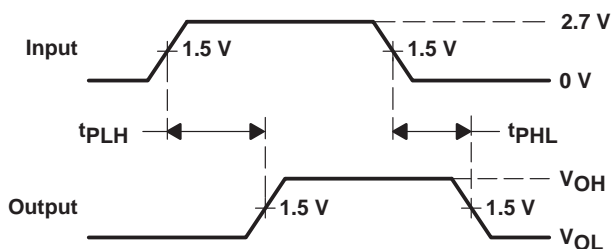


LOAD CIRCUIT

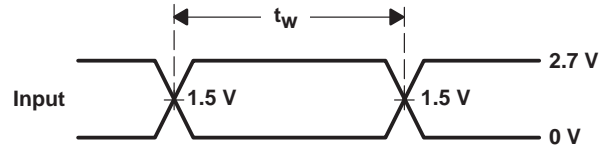
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



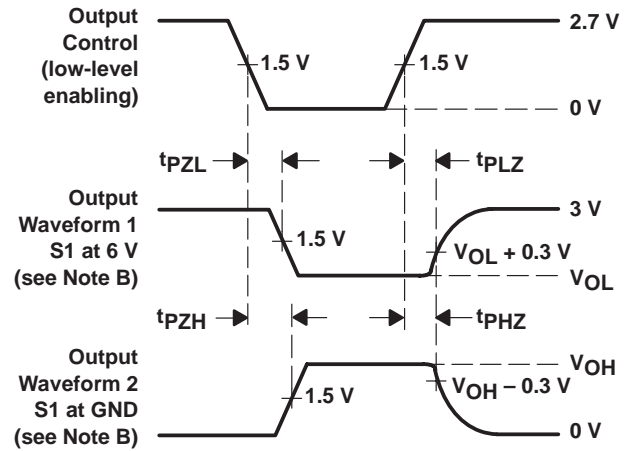
VOLTAGE WAVEFORMS
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Figure 3. Load Circuit and Voltage Waveforms

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