

74ABT573 Octal D-Type Latch with 3-STATE Outputs

General Description

The ABT573 is an octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

This device is functionally identical to the ABT373 but has broadside pinouts.

Features

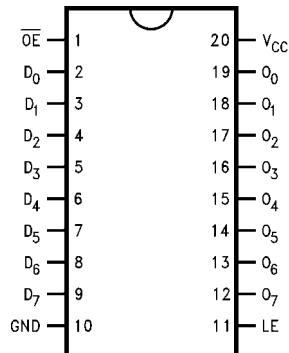
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to ABT373
- 3-STATE outputs for bus interfacing
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down
- Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT573CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT573CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT573CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT573CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT573CPC	N20A	20-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-01, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Descriptions
D_0 – D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	3-STATE Output Enable Input (Active LOW)
O_0 – O_7	3-STATE Latch Outputs

Functional Description

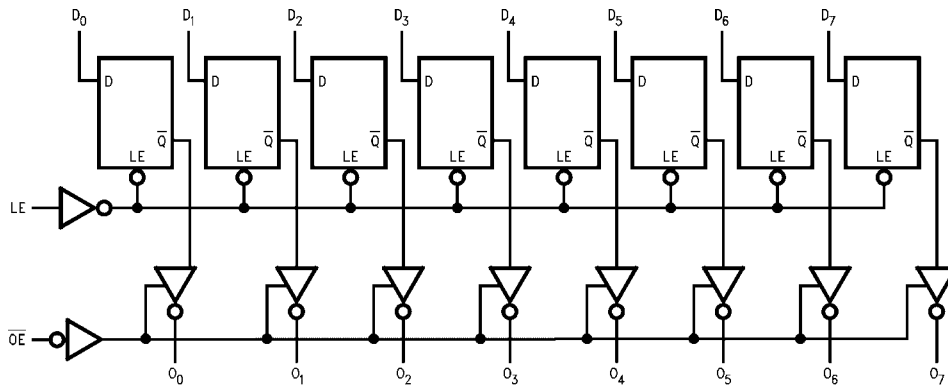
The ABT573 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
\overline{OE}	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 O_0 = Value stored from previous clock cycle

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to +5.5V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	Twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.5			V	Min	I _{OH} = -3 mA I _{OH} = -32 mA
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current			1	μA	Max	V _{IN} = 2.7V (Note 4) V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-1	μA	Max	V _{IN} = 0.5V (Note 4) V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			10	μA	0 - 5.5V	V _{OUT} = 2.7V; \overline{OE} = 2.0V
I _{OZL}	Output Leakage Current			-10	μA	0 - 5.5V	V _{OUT} = 0.5V; \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	\overline{OE} = V _{CC} All Others at V _{CC} or GND
I _{CC1}	Additional I _{CC} /Input			2.5	mA	Max	V _I = V _{CC} - 2.1V Enable Input V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND
I _{CC2}	Dynamic I _{CC}	No Load		0.12	mA/ MHz	Max	Outputs Open \overline{OE} = GND, LE = V _{CC} (Note 3) One Bit Toggling, 50% Duty Cycle

Note 3: For 8 bits toggling, I_{CC2} < 0.8 mA/MHz.

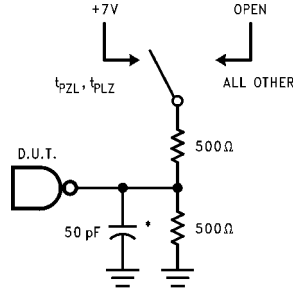
Note 4: Guaranteed but not tested.

DC Electrical Characteristics							
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.7	1.0	V	5.0	T _A = 25°C (Note 5)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-1.5	-1.2		V	5.0	T _A = 25°C (Note 5)
V _{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T _A = 25°C (Note 6)
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.2	1.8		V	5.0	T _A = 25°C (Note 7)
V _{ILD}	Maximum LOW Level Dynamic Input Voltage		1.0	0.7	V	5.0	T _A = 25°C (Note 7)
<p>Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.</p> <p>Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.</p> <p>Note 7: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.</p>							
AC Electrical Characteristics							
(SOIC and SSOP Package)							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	1.9	2.7	4.5	1.9	4.5	ns
t _{PHL}	D _n to O _n	1.9	2.8	4.5	1.9	4.5	
t _{PLH}	Propagation Delay	2.0	3.1	5.0	2.0	5.0	ns
t _{PHL}	LE to O _n	2.0	3.0	5.0	2.0	5.0	
t _{PZH}	Output Enable Time	1.5	3.1	5.3	1.5	5.3	ns
t _{PZL}		1.5	3.1	5.3	1.5	5.3	
t _{PHZ}	Output Disable Time	2.0	3.6	5.4	2.0	5.4	ns
t _{PLZ}	Time	2.0	3.4	5.4	2.0	5.4	
AC Operating Requirements							
(SOIC and SSOP Package)							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{TOGGLE}	Max Toggle Frequency		100				MHz
t _{S(H)}	Set Time, HIGH	1.5			1.5		ns
t _{S(L)}	or LOW D _n to LE	1.5			1.5		
t _{H(H)}	Hold Time, HIGH	1.0			1.0		ns
t _{H(L)}	or LOW D _n to LE	1.0			1.0		
t _{W(H)}	Pulse Width, LE HIGH	3.0			3.0		ns

Extended AC Electrical Characteristics								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 8)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ (Note 9)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 10)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	5.2	2.0	6.8	2.0	9.0	ns
t_{PHL}	D_n to O_n	1.5	5.2	2.0	6.8	2.0	9.0	
t_{PLH}	Propagation Delay	1.5	5.5	2.0	7.5	2.0	9.5	ns
t_{PHL}	LE to O_n	1.5	5.5	2.0	7.5	2.0	9.5	
t_{PZH}	Output Enable Time	1.5	6.2	2.0	8.0	2.0	10.5	ns
t_{PZL}		1.5	6.2	2.0	8.0	2.0	10.5	
t_{PHZ}	Output Disable Time	1.0	5.5	(Note 11)		(Note 11)		ns
t_{PLZ}		1.0	5.5	(Note 11)		(Note 11)		
<p>Note 8: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p>Note 9: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.</p> <p>Note 10: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p>Note 11: The 3-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.</p>								
Skew								
(Note 12)								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 12)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 13)				Units
		Max	Max	Max	Max			
t_{OSHL} (Note 14)	Pin to Pin Skew, HL Transitions	1.0		1.5				ns
t_{OSLH} (Note 14)	Pin to Pin Skew, LH Transitions	1.0		1.5				ns
t_{PS} (Note 15)	Duty Cycle, LH-HL Skew	1.4		3.5				ns
t_{OST} (Note 14)	Pin to Pin Skew, LH/HL Transitions	1.5		3.9				ns
t_{PV} (Note 16)	Device to Device Skew LH/HL Transitions	2.0		4.0				ns
<p>Note 12: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p>Note 13: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p>Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). This specification is guaranteed but not tested.</p> <p>Note 15: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.</p> <p>Note 16: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.</p>								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions ($T_A = 25^\circ\text{C}$)				
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$				
C_{OUT} (Note 17)	Output Capacitance	9	pF	$V_{CC} = 5.0\text{V}$				
<p>Note 17: C_{OUT} is measured at frequency $f = 1\text{ MHz}$ per MIL-STD-883B, Method 3012.</p>								

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Test Load

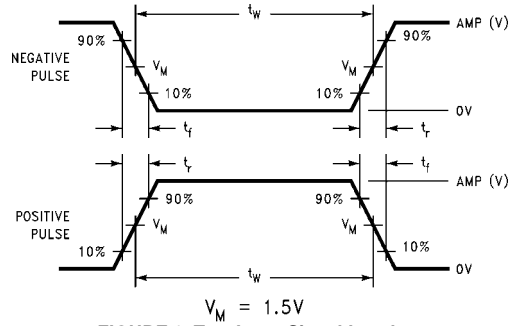


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

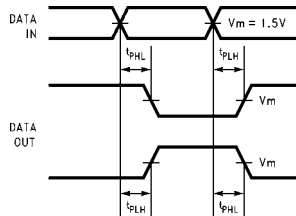


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

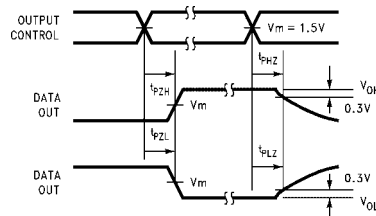


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

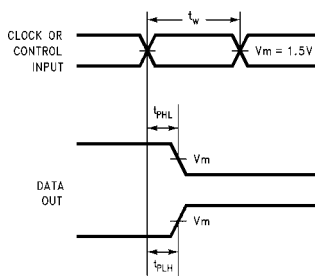


FIGURE 5. Propagation Delay, Pulse Width Waveforms

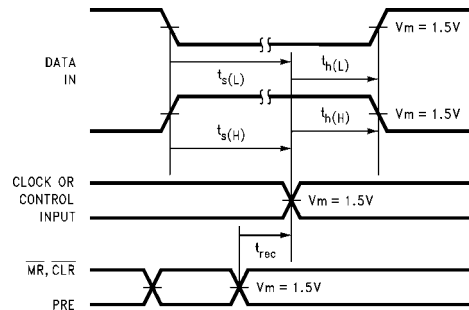
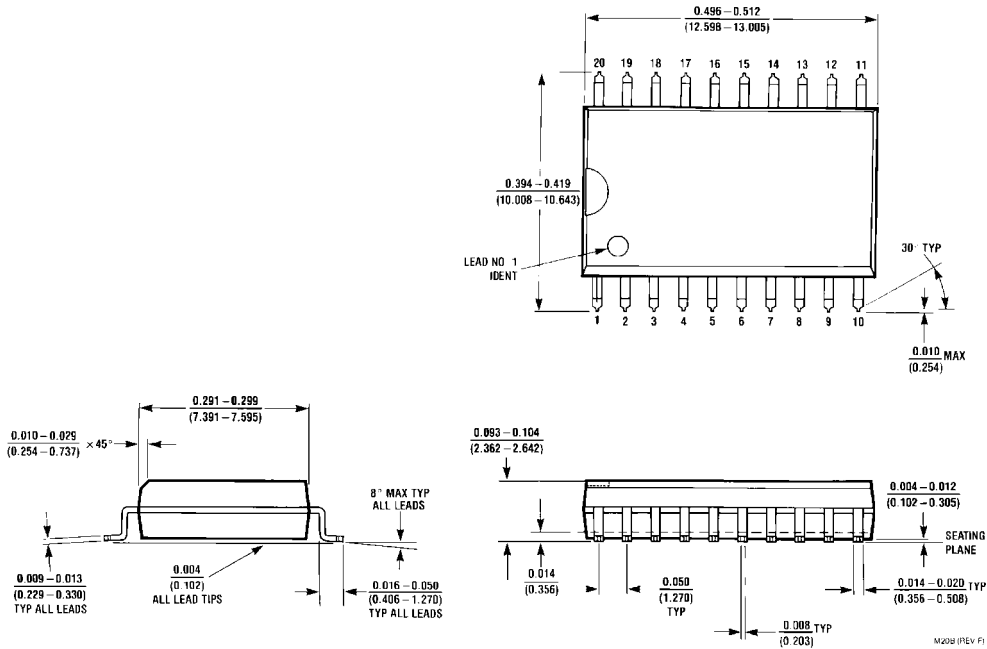


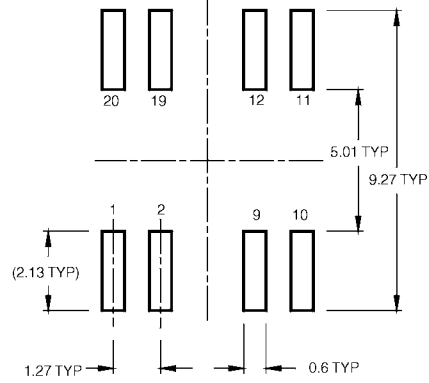
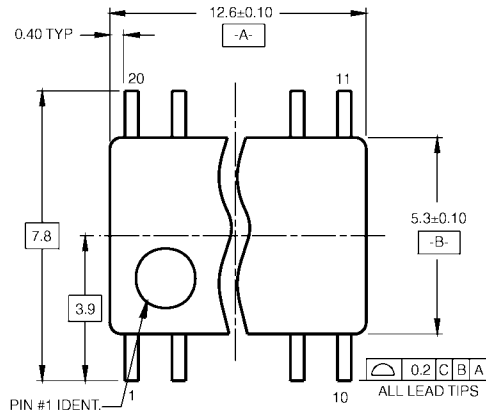
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

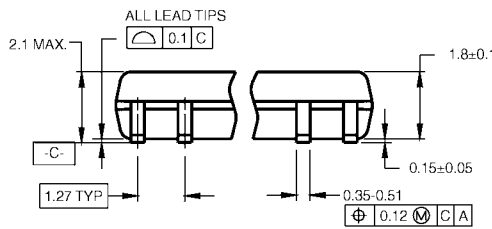


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B**

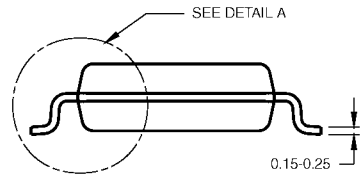
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



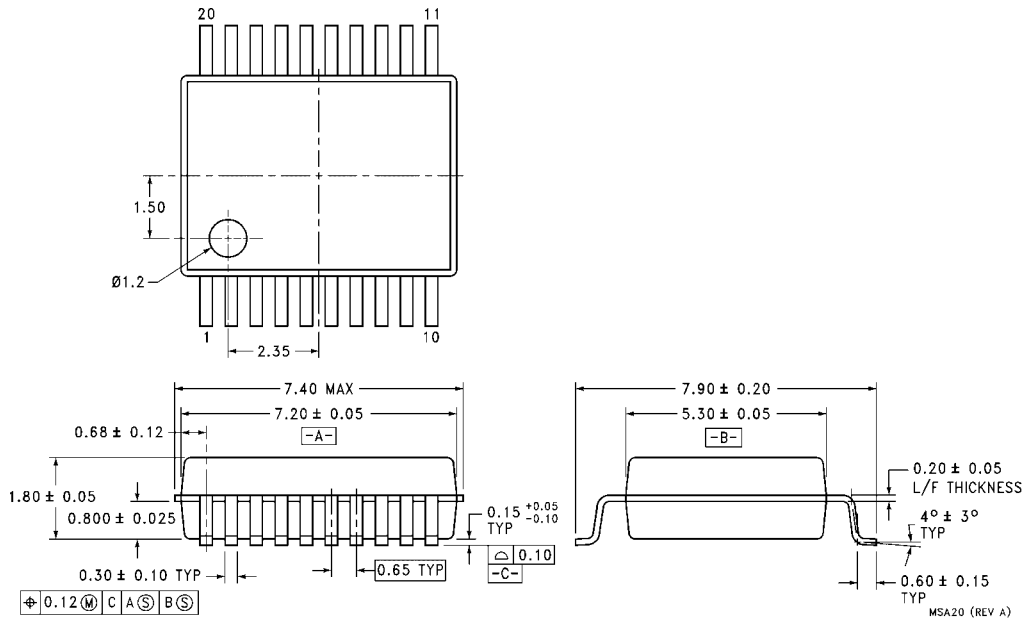
DETAIL A

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

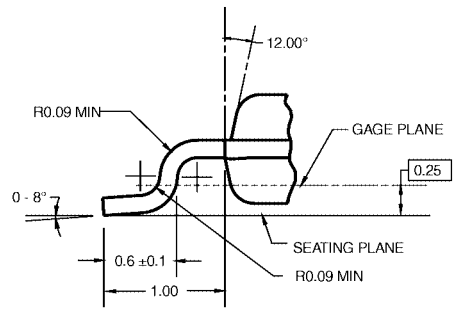
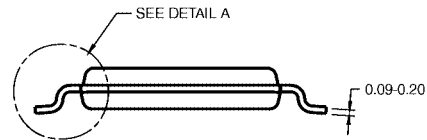
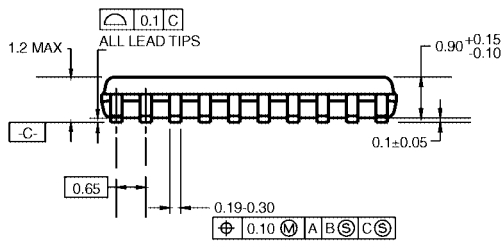
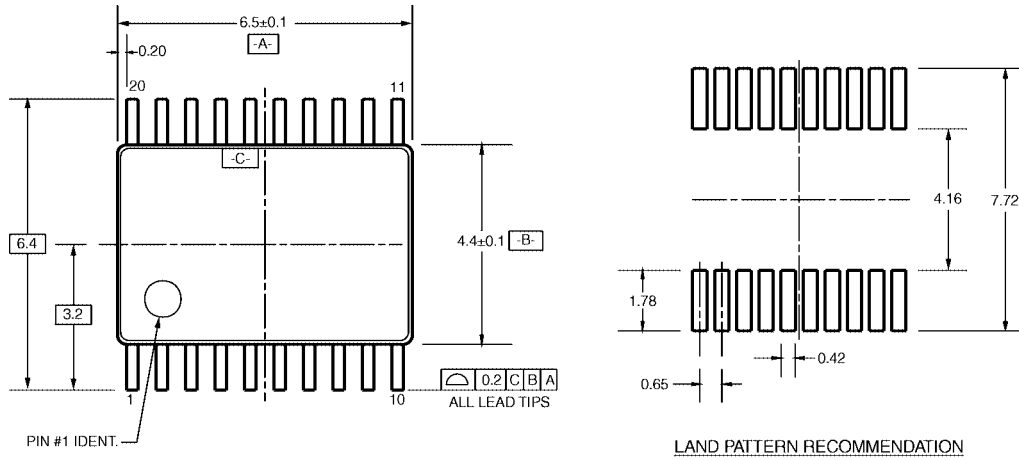
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

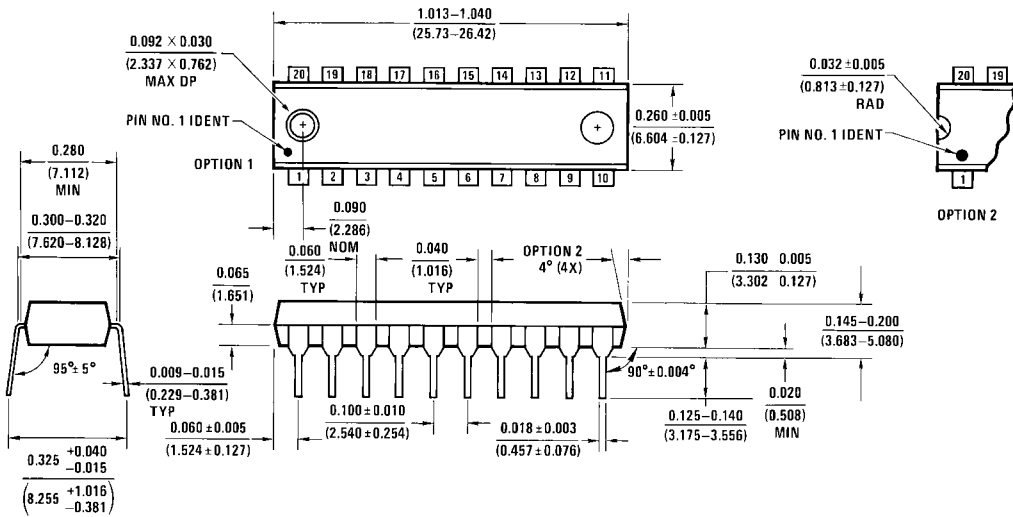


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-01, 0.300" Wide
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com