1-10 Clock Buffer for Networking Applications

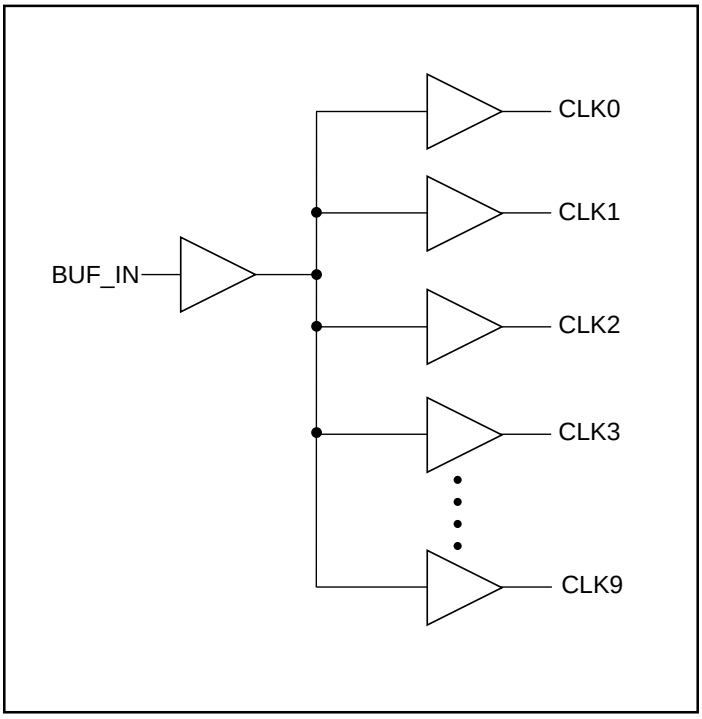
Product Features

- High Frequency >156 MHz
- High-speed, low-noise, non-inverting 1-10 buffer
- Low-skew (<250ps) between any two output clocks
- Low duty cycle distortion <250ps
- Low propagation delay <2.5ns
- Multiple V_{DD}, GND pins for noise reduction
- 3.3V supply voltage
- Available in SOIC, SSOP, and QSOP packages

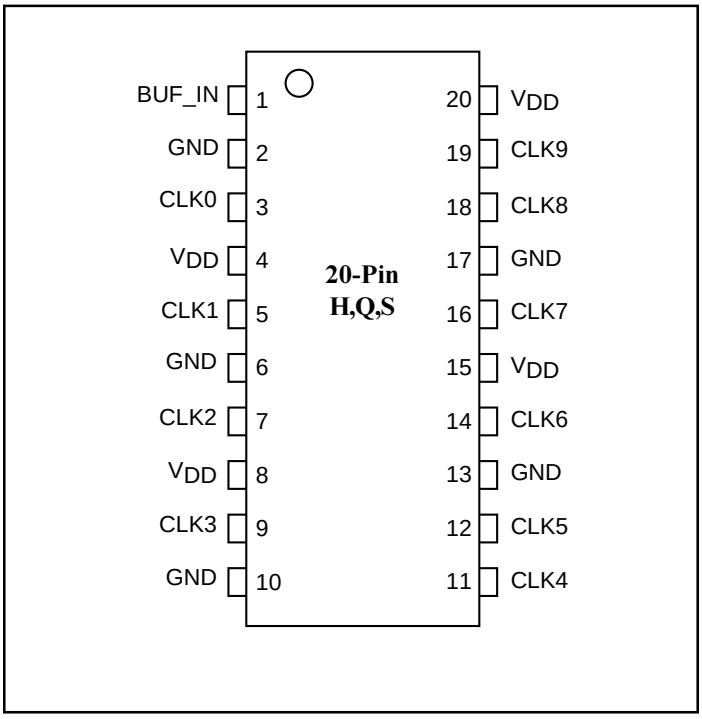
Description

The PI49FCT3807D is a 3.3V compatible, high-speed, low-noise 1-10 non-inverting clock buffer. The key goal in designing the PI6C3807D is to target networking applications that require low-skew, low-jitter, and high-frequency clock distribution. Providing output-to-output skew as low as 150ps, the PI49FCT3807D is an ideal clock distribution device for synchronous systems. Designing synchronous networking systems requires a tight level of skew from a large number of outputs.

Block Diagram



Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
V_{DD} Voltage	–0.5V to +4.6V
Output Voltage	–0.5V to V_{DD}+0.5V
Input Voltage	–0.5V to +7.0V
DC Output Current	–60mA to +60mA
Power Dissipation	500mW

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

V_{DD} Voltage	3.3V±0.3V
Commercial Temperature	–0°C to +70°C
Industrial Temperature	–40V to +85V
Input Frequency	DC to 156 MHz
Capacitive Loading	10pF to 50pF

DC Electrical Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level (Input Pins)		2.0	—	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level (Input Pins)		–0.5	—	0.8	
I_{IH}	Input HIGH Current	V_{DD} = Max.	V_{IN} = V_{DD}	—	—	1	µA
I_{IL}	Input LOW Current	V_{DD} = Max.	V_{IN} = GND	—	—	–1	
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –0.1mA	V_{DD} –0.2	—	—	
			I_{OH} = –12mA	2.4[3]	3.0	—	
V_{OL}	Output LOW Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	—	—	0.2	
			I_{OL} = 12mA	—	0.3	0.5	
I_{OH}	Output HIGH Current	V_{DD} = 3.0V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		–45	–75	–180	mA
I_{OL}	Output LOW Current	V_{DD} = 3.0V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		50	92	200	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. V_{OH} = V_{CC} – 0.6V at rated current.
4. This parameter is determined by device characterization but is not production tested.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max.	V_{IN} = GND or V_{DD}	—	0.1	30	µA
ΔI_{DD}	Supply Current per Inputs @ TTL HIGH	V_{DD} = Max.	V_{IN} = V_{DD} – 0.6V[3]	—	47	300	
I_{DD}	Dynamic Supply Current	V_{DD} = 3.6V, No Load	50 MHz	—	43	—	mA
			67 MHz	—	56	—	
			80 MHz	—	66	—	
			100 MHz	—	81	—	
			125 MHz	—	97	—	
			156 MHz	—	121	—	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{DD} = 3.3V, +25°C ambient.
3. Per TTL driven input (V_{IN} = V_{DD} – 0.6V); all other inputs at V_{DD} or GND.

Capacitance (T_A = 25°C, f = 1 MHz)

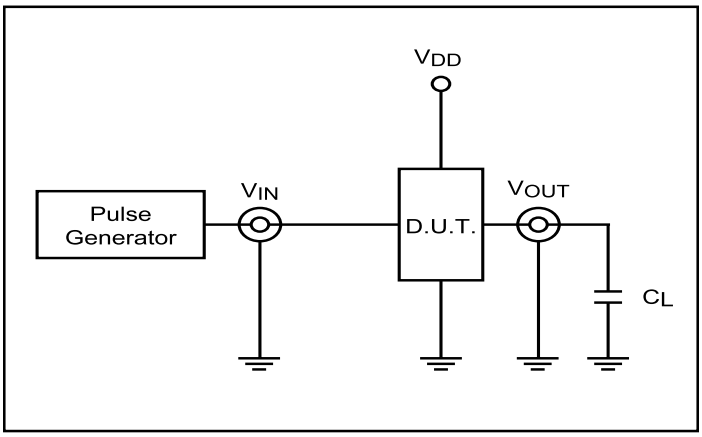
Parameters[1]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	3.0	4	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	6	

Note:
1. This parameter is determined by device characterization but is not production tested.

Product Pin Description

Pin Name	Description
BUF_IN	Input
CLK[0:9]	Outputs
GND	Ground
V_{DD}	Power

Test Circuits for All Outputs



Definitions:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Zout of the Pulse Generator.

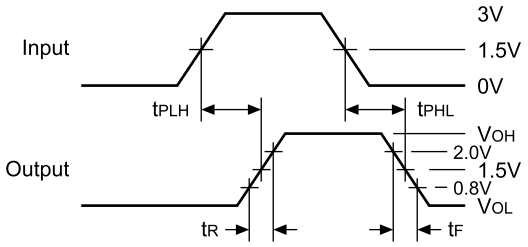
Switching Characteristics (V_{CC} = 3.3V ± 0.3V, T_A = 85°C)

Parameters	Description	Test Conditions(1)	Min.	Typ.	Max.	Units
tR/tF	CLKn Rise/Fall Time 0.8V~2.0V	C_L = 15pF, 125 MHz	–	0.7	1.0	ns
t_{PLH} t_{PHL}	Propagation Delay BUF_IN to CLKn	C_L = 15pF, 125 MHz	1.0	2.2	2.5	
$t_{SK(o)}$(3)	Skew between two outputs of the same package (same transition)	C_L = 15pF, 125 MHz	–	110	250	ps
$t_{SK(p)}$(3)	Skew between opposite transitions (t_{PHL}-t_{PLH}) of the same output	C_L = 15pF, 125 MHz	–	200	250	
$t_{SK(t)}$(3)	Skew between two outputs of different package (4)	C_L = 15pF, 125 MHz	–	–	0.55	ns

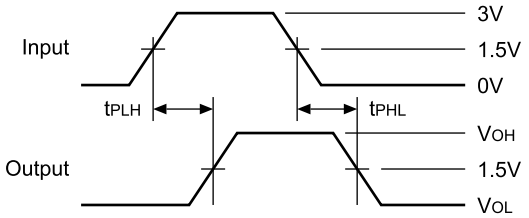
Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.

SWITCHING WAVEFORMS

Propagation Delay

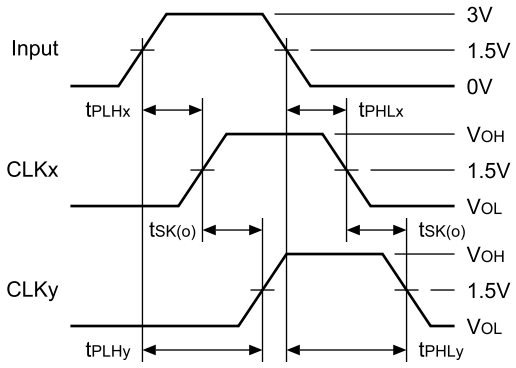


Pulse Skew – $t_{SK(P)}$



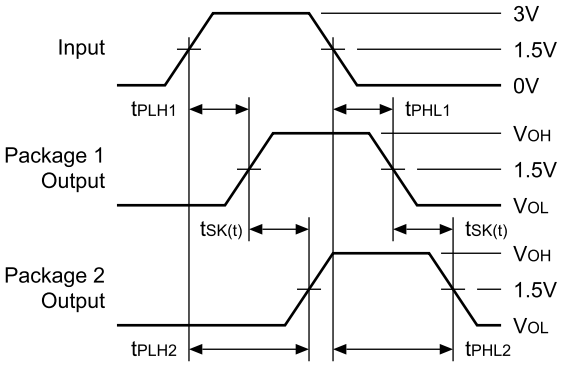
$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Output Skew – $t_{SK(O)}$



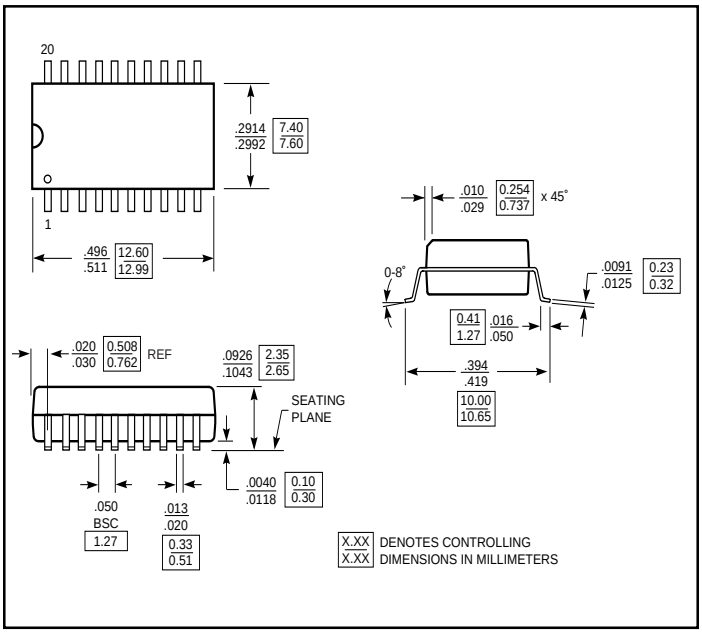
$t_{SK(o)} = |t_{PLHy} - t_{PLHx}|$ or $|t_{PHLy} - t_{PHLx}|$

Package Skew – $t_{SK(T)}$

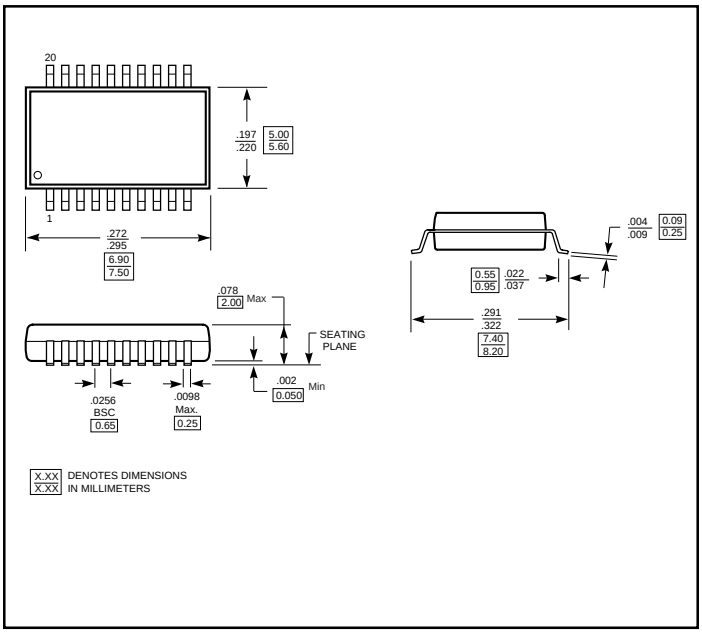


$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

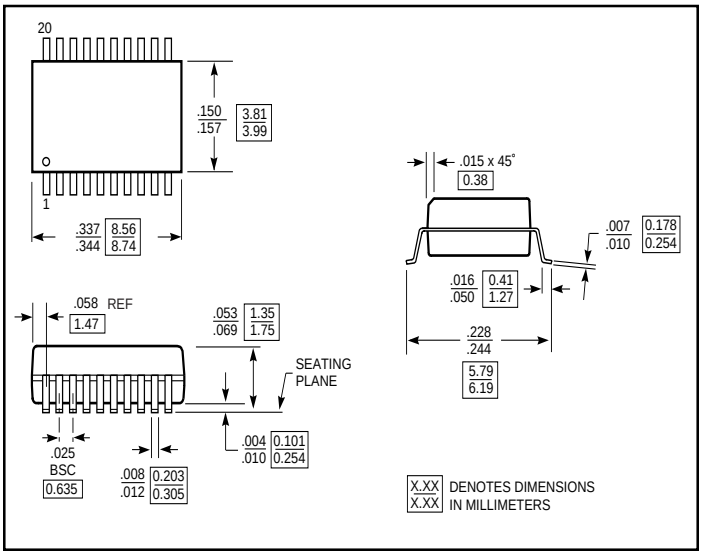
20-Pin SOIC (S20) Package



20-Pin SSOP (H20) Package



20-Pin QSOP (Q20) Package



Ordering Information

Ordering Code	Package Type
PI49FCT3807DS	20-pin 300 mil wide SOIC
PI49FCT3807DQ	20-pin 150 mil wide QSOP
PI49FCT3807DH	20-pin 209 mil wide SSOP